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(54) SOLID-STATE IMAGE PICKUP DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a solid-state image pickup device capable of preventing the fluctuation of the loads of a vertical shift register for read and the vertical shift register for an electronic shutter in the case of performing an electronic shutter operation and preventing the generation of image noise such as horizontal stripes on the display screen of output signals.

SOLUTION: This device is provided with an image pickup area where a unit cell provided with a photodiode PD to be a pixel is two-dimensionally arranged, plural read lines 4 for driving the read transistor Td of each pixel row, plural vertical selection lines 6 for driving the vertical selection transistor Ta of each of the pixel rows, a vertical driving circuit 24 for selectively driving the plural read lines 4 and selectively driving the plural vertical selection lines 6, plural vertical signal lines VLIN for outputting signals from each unit cell of the successively driven pixel rows and row selection circuits 2, 21 and 22 for controlling the vertical driving circuit so as to successively drive the read transistor Td of each pixel two times at a desired signal storage timing and a signal read timing and to drive the vertical selection transistor Ta of the pixel row at the signal read timing.

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19 CLAIMS

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21 [Claim(s)]

22 [Claim 1] A photo-electric-conversion means to carry out photo electric conversion of the
23 incident light to a pixel, and to accumulate a charge, the read-out means which reads the
24 accumulated charge to a detecting element, It comes to arrange the unit cell which has the
25 perpendicular selection means to which a signal is made to output from the resetting
26 means and said magnification means for resetting the charge of a magnification means to
27 amplify the read charge, and said detecting element on a semi-conductor substrate two-

1 dimensional. The image pick-up field which has a pixel line for two or more signal read-
2 out, and at least two dummy pixel lines, Two or more read lines for transmitting the read-
3 out driving signal for driving each read-out means of the unit cell of a pixel line which is
4 horizontally prepared corresponding to each pixel line in said image pick-up field, and
5 corresponds, respectively, Two or more perpendicular selection lines for transmitting the
6 line selection driving signal for driving each perpendicular selection means of the unit
7 cell of a pixel line which is horizontally prepared corresponding to each pixel line in said
8 image pick-up field, and corresponds, respectively, said -- more than one are read to the
9 read line of a book, a driving signal is supplied alternatively, and said read-out means is
10 driven -- both with the vertical-drive means for [said] supplying alternatively two or
11 more line selection driving signals to the perpendicular selection line of a book, and
12 driving said perpendicular selection means A line selection means to control said vertical-
13 drive means to make the read-out means of each pixel line in said image pick-up field
14 drive twice one by one to desired signal are recording timing and signal read-out timing,
15 It is prepared corresponding to each pixel train in said image pick-up field, and two or
16 more perpendicular signal lines for transmitting perpendicularly the signal outputted,
17 respectively from each unit cell of the pixel line by which the sequential drive was
18 carried out with said vertical-drive means are provided. After said line selection means
19 controls signal read-out from the unit cell of the pixel line for said two or more signal
20 read-out by said vertical-drive means, A selection control is carried out so that the 1st
21 dummy pixel line of said two dummy pixel lines may be made to drive. The solid state
22 camera characterized by carrying out a selection control so that the 2nd dummy pixel line
23 of said said two dummy pixel lines may be made to drive after controlling the signal are
24 recording in the unit cell of the pixel line for said two or more signal read-out by said
25 vertical-drive means.

26 [Claim 2] In a solid state camera according to claim 1 said line selection means The shift
27 register for the electronic shutters for controlling the initiation period of the signal are
28 recording in said unit cell, It has a shift register for read-out for controlling the initiation
29 period of signal read-out from said unit cell. Said 1st dummy pixel line It is the solid state
30 camera which a selection control is carried out with the shift register for said read-out,
31 and is characterized by carrying out the selection control of said 2nd dummy pixel line
32 with the shift register for said electronic shutters.

33 [Claim 3] A photo-electric-conversion means to carry out photo electric conversion of the
34 incident light to a pixel, and to accumulate a charge, the read-out means which reads the
35 accumulated charge to a detecting element, It comes to arrange the unit cell which has the
36 perpendicular selection means to which a signal is made to output from the resetting
37 means and said magnification means for resetting the charge of a magnification means to
38 amplify the read charge, and said detecting element on a semi-conductor substrate two-
39 dimensional. Corresponding to each pixel line in the image pick-up field which has two
40 or more pixel lines, and said image pick-up field, it is prepared horizontally. Two or more
41 read lines for transmitting the read-out driving signal for driving each read-out means of
42 the unit cell of a pixel line which corresponds, respectively, Two or more perpendicular
43 selection lines for transmitting the line selection driving signal for driving each
44 perpendicular selection means of the unit cell of a pixel line which is horizontally
45 prepared corresponding to each pixel line in said image pick-up field, and corresponds,
46 respectively, said -- more than one are read to the read line of a book, a driving signal is

1 supplied alternatively, and said read-out means is driven -- both with the vertical-drive
2 means for [said] supplying alternatively two or more line selection driving signals to the
3 perpendicular selection line of a book, and driving said perpendicular selection means A
4 line selection means to control said vertical-drive means to make the read-out means of
5 each pixel line in said image pick-up field drive twice one by one to desired signal are
6 recording timing and signal read-out timing, It is prepared corresponding to each pixel
7 train in said image pick-up field, and two or more perpendicular signal lines for
8 transmitting perpendicularly the signal outputted, respectively from each unit cell of the
9 pixel line by which the sequential drive was carried out with said vertical-drive means are
10 provided. 1st means by which said line selection means makes the read-out means of
11 each of said pixel line drive to said signal read-out timing with said vertical-drive means,
12 The solid state camera characterized by providing 2nd at least two means to make the
13 read-out means of each of said pixel line drive to said signal are recording timing with
14 said vertical-drive means.

15 [Claim 4] In a solid state camera according to claim 3 said image pick-up field At least
16 three dummy pixel lines other than said two or more pixel lines for signal read-out are
17 provided further. Said line selection means The solid state camera characterized by
18 making one dummy pixel line in said dummy pixel line drive with said 1st means, and
19 making other two dummy pixel lines in said dummy pixel line drive with said 2nd two
20 means.

21 [Claim 5] It is the solid state camera characterized by changing the signal are recording
22 timing within the period of 1 field period in 1 field unit on a solid state camera according
23 to claim 3 or 4 and corresponding to the period of the signal read-out timing of each pixel
24 line in said line selection means.

25 [Claim 6] It is the solid state camera characterized by for said 2nd at least two means
26 changing relatively the signal are recording timing to said signal read-out timing mutually
27 in a solid state camera according to claim 5, making said read-out means drive, and
28 switching the control action of said vertical-drive means by said 2nd means by turns for
29 every field.

30 [Claim 7] In a solid state camera according to claim 5 the 1st means of said line selection
31 means The shift register for read-out for controlling the initiation period of signal read-
32 out from said unit cell is provided. The 2nd means of said line selection means The
33 initiation period of the signal are recording in said unit cell in the shift register for the 1st
34 electronic shutter for controlling the initiation period of the signal are recording in said
35 unit cell in the 1st field period and the 1st [said] field period, and the 2nd field period
36 repeated by turns The solid state camera characterized by providing the shift register for
37 the 2nd electronic shutter for controlling.

38 [Claim 8] It is the solid state camera characterized by controlling said vertical-drive
39 means to make the same substantially the electrical potential difference of other wiring
40 which adjoins said read line around said photo-electric-conversion means also with the
41 time of said two drives in case said line selection means makes the read-out means of
42 each pixel line in said image pick-up field drive twice in claim 1 thru/or the solid state
43 camera of any one publication of seven .

44 [Claim 9] Other wiring which adjoins said read line in a solid state camera according to
45 claim 8 is solid state cameras characterized by being said perpendicular selection line.

46 [Claim 10] When reading stored charge from the optoelectric transducer of the unit cell

1 arranged two-dimensional to the image pick-up field on a semi-conductor substrate, In
2 the solid state camera which performs electronic shutter actuation to which the signal
3 which was made to drive twice one by one to the signal are recording timing and signal
4 read-out timing of a request of wiring which controls this read-out, and was read to said
5 signal read-out timing is made to output The solid state camera characterized by making
6 the same substantially the electrical potential difference of other wiring which adjoins
7 wiring which controls said read-out and exists around said optoelectric transducer to said
8 signal are recording timing and signal read-out timing.

9 [Claim 11] In claim 1 thru/or the solid state camera of any one publication of ten said unit
10 cell One read-out transistor to which the end side was connected to the cathode side of
11 the photodiode which is one piece by which touch-down potential is given to an anode
12 side, and said one photodiode, it read to the gate and the line was connected, One
13 magnification transistor by which the gate was connected to the other end side of said
14 read-out transistor, and the perpendicular signal line was connected to the end side, One
15 perpendicular selection transistor by which the end side was connected to the other end
16 side of said magnification transistor, and the perpendicular selection line was connected
17 to the gate, It connects between one power-source line connected to the other end side of
18 said perpendicular selection transistor, and the gate of said magnification transistor and
19 said power-source line. The solid state camera characterized by providing in the gate one
20 reset transistor to which the reset line was connected, and said one photodiode
21 corresponding to one pixel.

22 [Claim 12] The solid state camera characterized by to be at the each pixel's read-out time,
23 and to make the same substantially the electrical potential difference of other wiring
24 which adjoins wiring which controls this read-out and exists around said optoelectric
25 transducer in case the unit cell of 2 pixels / 1 unit reads stored charge from the 2-pixel
26 optoelectric transducer in the unit cell of said image pick-up field in the solid state
27 camera which has the image pick-up field which it comes to arrange on a semi-conductor
28 substrate two-dimensional, respectively.

29 [Claim 13] In claim 1 thru/or the solid state camera of any one publication of 12 said unit
30 cell One one end each is connected to each anode side respectively corresponding to each
31 cathode side of the photodiode which is two pieces to which touch-down potential is
32 given, and said two photodiodes. Two read-out transistors to which two read lines were
33 connected respectively corresponding to each gate, One magnification transistor by
34 which the gate was connected common to each said two other end side of a read-out
35 transistor, and the perpendicular signal line was connected to the end side, One
36 perpendicular selection transistor by which the end side was connected to the other end
37 side of said magnification transistor, and said perpendicular selection line was connected
38 to the gate, It connects between one power-source line connected to the other end side of
39 said perpendicular selection transistor, and the gate of said magnification transistor and
40 said power-source line. The solid state camera characterized by providing in the gate one
41 reset transistor to which the reset line was connected, and said two photodiodes
42 corresponding to two pixels.

43 44 DETAILED DESCRIPTION 45

1 [Detailed Description of the Invention]
2 [0001]
3 [Field of the Invention] This invention relates to a solid state camera, especially is used
4 for a video camera, an electronic still camera, etc. about the good transformation child
5 shutter control circuit of a solid state camera, and a pixel signal read-out control circuit.
6 [0002]
7 [Description of the Prior Art] Drawing 12 shows the equal circuit of the CMOS solid
8 state camera (magnification mold CMOS image sensors) of the conventional example 1
9 equipped with the readout circuitry which a pixel signal can read for every pixel.
10 [0003] In drawing 12 , the unit cell of 1 pixel (1 pixel) / 1 unit is arranged in the shape of
11 [which is two dimensions] a matrix, and is formed in the cel field (image pick-up field).
12 [0004] Each unit cell consists of four transistors Ta, Tb, Tc, and Td and one photodiode
13 PD.
14 [0005] Namely, the photodiode PD with which touch-down potential is given to an anode/
15 side The read-out transistor Td by which the end side is connected to the cathode side of
16 Photodiode PD (shutter gate transistor), The magnification transistor Tb by which the
17 gate is connected to the other end side of the read-out transistor Td The reset transistor Tc
18 by which the end side is connected to the gate of the perpendicular selection transistor
19 (line selection transistor) Ta and the magnification transistor Tb where the end side is
20 connected to the end side of the magnification transistor Tb is provided.
21 [0006] And corresponding to each pixel line, the perpendicular selection [which was
22 connected common to the gate of each read-out transistor Td of the unit cell of the same
23 line] line 6 connected with the line 4 common to the gate of each perpendicular selection
24 transistor Ta of the unit cell of the same line and the reset line 7 connected common to
25 the gate of each reset transistor Tc of the unit cell of the same line are formed in said cel
26 field by reading.
27 [0007] Moreover, corresponding to each pixel train, the power-source line 9 connected
28 common to the other end [of each reset transistor Tc of the unit cell of the same train as
29 the perpendicular signal line VLIN connected common to the other end side of each
30 magnification transistor Tb of the unit cell of the same train] and other end side of each
31 perpendicular selection transistor Ta is formed in said cel field.
32 [0008] Furthermore, in the exterior by the side of the end of a cel field, two or more load
33 transistors TL connected, respectively between one one end each of said perpendicular
34 signal line VLIN and a touch-down node are arranged horizontally.
35 [0009] Moreover, in the exterior by the side of the other end of a cel field, two or more
36 noise canceller circuits which consisted of two transistors TSH and TCLP and two
37 capacitors Cc and Ct are arranged horizontally.
38 [0010] And two or more level selection transistors TH connected to each other end side
39 of said perpendicular signal line VLIN through each above-mentioned noise canceller
40 circuit are arranged horizontally.
41 [0011] The level signal line HLIN is connected to each other end of the above-mentioned
42 level selection transistor TH in common, and they are a level reset transistor (not shown)
43 and the output amplifying circuit AMP in this level signal line HLIN. It connects.
44 [0012] In addition, the transistor TSH for sample hold by which, as for said each noise
45 canceller circuit, the end side was connected to the other end side of the perpendicular
46 signal line VLIN Coupling-capacitor Cc by which the end side was connected to the other

1 end side of the transistor TSH for these sample hold, The capacitor Ct for charge storages
2 connected between touch-down nodes the other end side of this coupling-capacitor Cc, It
3 is constituted by the transistor TCLP for a potential clamp connected to the connection
4 node of said capacitors Cc and Ct, and the end side of said level selection transistor TH is
5 connected to the connection node of said capacitors Cc and Ct.
6 [0013] furthermore, in the exterior of a cel field Two or more perpendicular selection
7 lines 6 of a cel field The timing generating circuit 10 which generates various kinds of
8 timing signals for supplying the perpendicular shift register 2 for carrying out a selection
9 control in scan, and said level selection transistor TH to the level shift register 3 for
10 driving in scan, said noise canceller circuit, etc., The bias generating circuit 11 for
11 generating predetermined bias potential at the end of the transistor TCLP for the potential
12 clamp of said noise canceller circuit etc., Pulse selector 2a for carrying out the selection
13 control of the output pulse of the above-mentioned perpendicular shift register 2, and
14 driving the perpendicular selection line 6 of each line of a cel field in scan is arranged,
15 respectively.
16 [0014] Drawing 13 is the timing wave form chart showing an example of actuation of the
17 solid-state image sensors shown in drawing 12 .
18 [0015] Next, actuation of the solid-state image sensors of drawing 12 is explained,
19 referring to drawing 13 .
20 [0016] The signal charge which photo electric conversion of the incident light of each
21 photodiode PD was carried out, and it produced is accumulated into Photodiode PD.
22 [0017] In a horizontal blanking interval, in case the signal charge of Photodiode PD is
23 read from the unit cell for a certain party, in order to choose each perpendicular signal
24 line VLIN, the line selection transistor Ta for a party is first turned ON by turning ON the
25 signal (phiADRES pulse) of the perpendicular selection line 6 of the line for selection.
26 [0018] The source follower circuit which consists of a magnification transistor Tb to
27 which the power-source potential VDD (for example, 3.3V) is supplied through the line
28 selection transistor Ta, and a load transistor TL in the unit cell for said party by this is
29 operated.
30 [0019] Next, in the unit cell for said party, reference voltage is outputted to the
31 perpendicular signal line VLIN by turning ON the signal (phiRESET pulse) of the reset
32 line 7, and carrying out fixed period reset of the gate voltage of the magnification
33 transistor Tb at reference voltage.
34 [0020] However, as described above, dispersion exists in the gate potential of the reset
35 magnification transistor Tb, and dispersion appears also in the reset potential of the
36 perpendicular signal line VLIN by the side of the other end.
37 [0021] Then, in order to reset dispersion in the reset potential of each perpendicular
38 signal line VLIN The driving signal (phiSH pulse) of the transistor TSH for sample hold
39 in a noise canceller circuit is turned ON beforehand (for example, the aforementioned
40 phiADRES to ON and coincidence of a pulse). After reference voltage is outputted to
41 said perpendicular signal line VLIN, by making the driving signal (phiCLP pulse) of the
42 transistor TCLP for a potential clamp fixed time amount ON, reference voltage is set as
43 the connection node of the capacitors Cc and Ct of a noise canceller circuit.
44 [0022] Next, aforementioned phiRESET After turning off a pulse, by choosing the read
45 line 4 of a predetermined line and turning on the signal (phiREAD pulse), the read-out
46 transistor Td is turned ON and gate potential is changed by reading the stored charge of

1 Photodiode PD to the gate of the magnification transistor Tb. The magnification
2 transistor Tb outputs the voltage signal according to the variation of gate potential to the
3 corresponding perpendicular signal line VLIN and a noise canceller circuit.
4 [0023] Then, a level effective scan term period can also accumulate the signal component
5 (signal level from which the noise was removed) equivalent to the difference of the
6 reference voltage read as described above, and a signal level in the capacitor Ct for
7 charge storages by turning off phiSH pulse in a noise canceller circuit.
8 [0024] That is, the noise mixed in the preceding paragraph side from noise canceller
9 circuits, such as dispersion in the reset potential of each perpendicular signal line VLIN
10 resulting from a cel field, is removed.
11 [0025] And phiADRES By the perpendicular selection transistor's Ta being controlled by
12 the OFF state, and changing a unit cell into the condition of not choosing, a cel field and
13 each noise canceller circuit are electrically separated by turning OFF a pulse.
14 [0026] By making sequential ON the driving signal (phiH pulse) of the level selection
15 transistor TH at a next horizontal effective scan period, the level selection transistor TH
16 is turned on [sequential], the signal level of the connection node (signal preservation
17 node) of said capacitors Cc and Ct is read to the level signal line HLIN one by one, and it
18 is the output amplifying circuit AMP. It is amplified and outputs.
19 [0027] It sets in the above-mentioned actuation and is the electrical potential difference
20 VVLIN of the perpendicular signal line VLIN. Noise rejection actuation which becomes
21 the operating voltage Vm (about 1.5 V) of a source follower circuit and which was
22 described in addition above is performed for every read-out actuation for every horizontal
23 line at a horizontal blanking interval.
24 [0028] Drawing 14 is the timing wave form chart showing the timing generating circuit
25 10 in drawing 13 , the perpendicular shift register 2, and the example of pulse selector 2a
26 of operation.
27 [0029] Here, the case where the solid state camera of drawing 12 is used by 1 field = 1 /
28 30Hz (image of 30 frames per second which make the 1 field one frame) system is
29 shown.
30 [0030] The timing generating circuit 10 operates external input pulse signal phiVR and
31 phiHP orthopedically in a buffer circuit, and is pulse signal phiVRR of a field period.
32 Pulse signal phiHPV of a level period It inputs into said perpendicular shift register 2.
33 [0031] The perpendicular shift register 2 is pulse signal phiVRR. Pulse signal phiHPV
34 after an input clears all register outputs at the period of "L" level and makes it "L" level A
35 shift action is performed, and the output pulse signal ROi (i=--, n, n+1, --) is made into
36 "H" level one by one, and is inputted into said pulse selector 2a.
37 [0032] Pulse selector 2a activates the signal (phiADRES pulse) of the perpendicular
38 selection line 6, the signal (phiRESET pulse) of the reset line 7, and the signal (phiREAD
39 pulse) of the read line 4, as shown in drawing 13 to each line for selection, and it scans
40 the line for selection.
41 [0033] It is each output pulse signal ROi of the perpendicular shift register 2 for the solid
42 state camera of drawing 12 to carry out the selection control of the specific line for
43 selection, as described above. It outputs only once within 1 field period. That is, since
44 Photodiode PD performs signal read-out in the 1 field only once, the electronic shutter
45 actuation which controls light-receiving time amount equivalent is impossible by
46 controlling the signal storage time of Photodiode PD.

1 [0034] On the other hand, drawing 15 shows roughly the configuration of the CMOS /
2 solid state camera of the conventional example 2 in which electronic shutter actuation is
3 possible.

4 [0035] This solid state camera For example, the image pick-up field 14 where the pixel
5 cel 13 constituted as shown in drawing 12 has been arranged two-dimensional in the
6 shape of a matrix (photo-electric-conversion section), Two or more perpendicular signal
7 lines VLIN formed in the direction of a pixel train of said image pick-up field 14 Two or
8 more perpendicular selection lines 6 for read-out control for controlling to be formed in
9 the pixel line writing direction of said image pick-up field 14, and to read the photo-
10 electric-conversion signal of each pixel cel 13 to said two or more perpendicular signal
11 lines VLIN per pixel line, The 1st perpendicular selection circuitry 2 for carrying out a
12 selection control in scan to the timing of read-out of said two or more perpendicular
13 selection lines 6 for read-out control (perpendicular shift register for read-out), The level
14 selection transistor TH for choosing said perpendicular signal line VLIN, The level
15 selection circuitry 3 for carrying out the selection control of said level selection transistor
16 (level selection shift register), Output amplifying circuit AMP for outputting the signal
17 read to the level signal line HLIN and said level signal line HLIN for reading the signal
18 of said perpendicular signal line VLIN chosen with said level selection shift register 3 It
19 provides.

20 [0036] In addition, especially the point equipped with a load transistor as shown in
21 drawing 12, a noise canceller circuit, etc. around the image pick-up field 14 although not
22 illustrated is the same as that of the CMOS solid state camera of an example 1.

23 [0037] Furthermore, the vertical-drive circuit (not shown) which generates the driving
24 signal for driving alternatively said two or more perpendicular selection lines 6 for read-
25 out control based on the output of the 2nd perpendicular selection circuitry (perpendicular
26 shift register for electronic shutters) 15 for carrying out a selection control in scan and
27 said 1st perpendicular selection circuitry and the output of the 2nd perpendicular
28 selection circuitry to the timing of signal are recording of said two or more perpendicular
29 selection lines 6 for read-out control is provided.

30 [0038] That is, the perpendicular shift register 15 for electronic shutters is formed
31 independently [the perpendicular shift register 2 for read-out], and it is constituted so
32 that this perpendicular shift register 15 for electronic shutters as well as the perpendicular
33 shift register 2 for read-out may scan the line for selection to predetermined timing.

34 [0039] Thereby, the perpendicular shift register 2 for read-out and the perpendicular shift
35 register 15 for electronic shutters enable it to carry out the selection control of the
36 specific line for selection to 2 times of timing within 1 field period.

37 [0040] Therefore, when the perpendicular shift register 15 for electronic shutters carries
38 out the selection control of the line for selection and starts are recording of a pixel signal
39 before the twist from which the perpendicular shift register 2 for read-out carries out the
40 selection control of the line for selection, and reads a pixel signal to the perpendicular
41 signal line VLIN, the electronic shutter actuation which controls light-receiving time
42 amount equivalent is attained.

43 [0041] By the way, the CMOS solid state camera of drawing 15 which has one
44 perpendicular shift register 2 for read-out and one perpendicular shift register 15 for
45 electronic shutters which were described above For example, when making the good
46 transformation child shutter actuation to which light-receiving time amount is changed

equivalent by changing the signal storage time automatically according to the output level of a photo sensor perform. There is a problem of the difference of the signal storage time arising to pixel spacing, or changing the load of two perpendicular shift registers 2 and 15 to it according to the merits and demerits of the signal storage time.

[0042] This problem is explained below.

[0043] Drawing 16 shows an example in case the line selection timing of two perpendicular shift registers 2 and 15 in drawing 15 is immobilization.

[0044] As shown in drawing 16, the timing to which the perpendicular shift register 15 for electronic shutters performs line selection ahead of the perpendicular shift register 2 for read-out is being fixed, that is, the two above-mentioned perpendicular shift registers 2 and 15 of the time difference which performs line selection are always fixed.

[0045] Thus, when the line selection timing of two perpendicular shift registers 2 and 15 is immobilization, the perpendicular shift register 2 for read-out and the perpendicular shift register 15 for electronic shutters begin selection of return and the following frame to the first rank again, after it begins selection of a certain frame and the shift action from the first rank to a tail end (that is, the number of pixels of the perpendicular direction of a solid state camera) finishes.

[0046] Therefore, the solid state camera of drawing 15 has the problem of the difference of the signal storage time arising to pixel spacing, or changing the load of two perpendicular shift registers 2 and 15 to it according to the merits and demerits of the signal storage time, when making the good transformation child shutter actuation to which light-receiving time amount is changed equivalent by changing the signal storage time automatically according to the output level of a photo sensor perform.

[0047] Here, said problem is stated to a detail, referring to drawing 17 about the case where the merits and demerits of the time amount in which the perpendicular shift register 15 for electronic shutters changes the timing (timing of an electronic shutter) which performs line selection ahead of the perpendicular shift register 2 for read-out, and accumulates a pixel signal as concrete technique for changing the signal storage time are changed.

[0048] In drawing 17, a read-out control pulse is a signal which makes the shift action of the perpendicular shift register 2 for read-out start, and a good transformation child shutter control pulse is a signal which makes the shift action of the perpendicular shift register 15 for electronic shutters start.

[0049] (1) After starting the shift action of the perpendicular shift register 15 for electronic shutters by the control pulse of the electronic shutter generated to the timing t1 in drawing 17 on the occasion of selection of the 1st frame, before the shift action to a tail end finishes (before choosing all pixel lines), in order to choose the 2nd frame to the timing t3 in drawing 17, suppose that the electronic shutter pulse occurred. In this case, the perpendicular shift register 15 for electronic shutters is reset to the above-mentioned timing t3, and starts a shift action (line selection) from the first rank again.

[0050] Thereby, in case [at which it generated to the timing t2 in drawing 17] it reads, and the shift action of the perpendicular shift register 2 for read-out begins by the control pulse and said 1st frame is read, the difference of the signal storage time arises in the pixel line by which selection assignment was not carried out with the pixel line by which selection assignment was carried out with the perpendicular shift register 15 for electronic shutters which the shift action started to said timing t1.

1 [0051] Thus, if the difference of the signal storage time arises, when a read-out output
2 level is changed depending on the location of a pixel line and displays the output signal
3 of a solid state camera on the screen of an image display device, it will become the cause
4 which image noises, such as a lateral stripe, generate.

5 [0052] (2) in the timing t4 in drawing 17 , the shift action began to the selection line and
6 said timing t2 of the perpendicular shift register 15 for electronic shutters which the shift
7 action started to said timing t3 -- reading -- business -- since a total of two pixel lines of
8 the selection line of the perpendicular shift register 2 are chosen, these two pixel lines
9 serve as a load of two perpendicular shift registers 2 and 15.

10 [0053] on the other hand, in the timing t6 in drawing 17 , the selection line by the
11 perpendicular shift register 15 for electronic shutters which the shift action started to said
12 timing t3 did not already exist, but the shift action started it to the timing t5 in drawing 17
13 -- reading -- business -- since one pixel line is chosen with the perpendicular shift register
14 2, this one pixel line serves as a load of two perpendicular shift registers 2 and 15.

15 [0054] Thus, if the load of two perpendicular shift registers 2 and 15 is changed
16 depending on electronic shutter timing, the voltage variation of power-source Rhine of a
17 solid state camera is imitated, and it comes, and when the output signal of a solid state
18 camera is displayed on the screen of an image display device, a lateral stripe will be
19 generated, and it will become the cause which worsens image quality notably.

20 [0055] In addition, the problem of the difference of the signal storage time arising to
21 pixel spacing, or changing the load of two perpendicular shift registers 2 and 15 to it
22 according to the merits and demerits of the signal storage time which was described
23 above is produced not only the solid state camera of a CMOS mold but when making the
24 solid state camera of a CCD mold perform good transformation child shutter actuation.

25 [0056]

26 [Problem(s) to be Solved by the Invention] As described above, when changing the signal
27 storage time and making good transformation child shutter actuation perform, according
28 to the merits and demerits of the signal storage time, the difference of the signal storage
29 time arose to pixel spacing, or the load of the perpendicular shift register for read-out and
30 the perpendicular shift register for electronic shutters was changed, and the conventional
31 solid state camera had the problem of becoming the cause which image noises, such as a
32 lateral stripe, generate in the display screen of an output signal.

33 [0057] the case where it was made that this invention should solve the above-mentioned
34 trouble, and electronic shutter actuation is made to perform -- reading -- business --
35 fluctuation of the load of a perpendicular shift register and the perpendicular shift register
36 for electronic shutters can be prevented, and it aims at offering the solid state camera
37 which can prevent generating of image noises, such as a lateral stripe in the display
38 screen of an output signal.

39 [0058] moreover, the case where this invention makes the good transformation child
40 shutter actuation (continuation electronic shutter actuation) to which the signal storage
41 time of a pixel is changed per field perform -- reading -- business -- fluctuation of the
42 load of a perpendicular shift register and the perpendicular shift register for electronic
43 shutters can be prevented, and it aims at offering the solid state camera which can prevent
44 generating of image noises, such as a lateral stripe in the display screen of an output
45 signal.

46 [0059] Moreover, this invention aims at offering the solid state camera which can prevent

1 that the difference of the signal storage time arises to pixel spacing according to the
2 merits and demerits of the signal storage time, when making continuation electronic
3 shutter actuation perform.

4 [0060] Moreover, this invention aims at offering the solid state camera which can prevent
5 generating of image noises, such as a lateral stripe in the display screen of an output
6 signal, when making continuation electronic shutter actuation perform.

7 [0061] Moreover, in case this invention reads photo electric conversion and the
8 accumulated signal by the pixel, it aims at offering the solid state camera which can
9 prevent that a noise jumps in by capacity coupling from wiring of the pixel
10 circumference.

11 [0062]

12 [Means for Solving the Problem] A photo-electric-conversion means for the 1st solid
13 state camera of this invention to carry out photo electric conversion of the incident light
14 to a pixel, and to accumulate a charge, The read-out means which reads the accumulated
15 charge to a detecting element, a magnification means to amplify the read charge, It comes
16 to arrange the unit cell which has the perpendicular selection means to which a signal is
17 made to output from the resetting means and said magnification means for resetting the
18 charge of said detecting element on a semi-conductor substrate two-dimensional. The
19 image pick-up field which has a pixel line for two or more signal read-out, and at least
20 two dummy pixel lines, Two or more read lines for transmitting the read-out driving
21 signal for driving each read-out means of the unit cell of a pixel line which is horizontally
22 prepared corresponding to each pixel line in said image pick-up field, and corresponds,
23 respectively, Two or more perpendicular selection lines for transmitting the line selection
24 driving signal for driving each perpendicular selection means of the unit cell of a pixel
25 line which is horizontally prepared corresponding to each pixel line in said image pick-up
26 field, and corresponds, respectively, said -- more than one are read to the read line of a
27 book, a driving signal is supplied alternatively, and said read-out means is driven -- both
28 with the vertical-drive means for [said] supplying alternatively two or more line
29 selection driving signals to the perpendicular selection line of a book, and driving said
30 perpendicular selection means A line selection means to control said vertical-drive means
31 to make the read-out means of each pixel line in said image pick-up field drive twice one
32 by one to desired signal are recording timing and signal read-out timing, It is prepared
33 corresponding to each pixel train in said image pick-up field, and two or more
34 perpendicular signal lines for transmitting perpendicularly the signal outputted,
35 respectively from each unit cell of the pixel line by which the sequential drive was
36 carried out with said vertical-drive means are provided. After said line selection means
37 controls signal read-out from the unit cell of the pixel line for said two or more signal
38 read-out by said vertical-drive means, A selection control is carried out so that the 1st
39 dummy pixel line of said two dummy pixel lines may be made to drive. After controlling
40 the signal are recording in the unit cell of the pixel line for said two or more signal read-
41 out by said vertical-drive means, it is characterized by carrying out a selection control so
42 that the 2nd dummy pixel line of said said two dummy pixel lines may be made to drive.

43 [0063] A photo-electric-conversion means for the 2nd solid state camera of this invention
44 to carry out photo electric conversion of the incident light to a pixel, and to accumulate a
45 charge, The read-out means which reads the accumulated charge to a detecting element, a
46 magnification means to amplify the read charge, The image pick-up field which it comes

1 to arrange the unit cell which has the perpendicular selection means to which a signal is
2 made to output from the resetting means and said magnification means for resetting the
3 charge of said detecting element on a semi-conductor substrate two-dimensional, and has
4 two or more pixel lines, Two or more read lines for transmitting the read-out driving
5 signal for driving each read-out means of the unit cell of a pixel line which is horizontally
6 prepared corresponding to each pixel line in said image pick-up field, and corresponds,
7 respectively, Two or more perpendicular selection lines for transmitting the line selection
8 driving signal for driving each perpendicular selection means of the unit cell of a pixel
9 line which is horizontally prepared corresponding to each pixel line in said image pick-up
10 field, and corresponds, respectively, said -- more than one are read to the read line of a
11 book, a driving signal is supplied alternatively, and said read-out means is driven -- both
12 with the vertical-drive means for [said] supplying alternatively two or more line
13 selection driving signals to the perpendicular selection line of a book, and driving said
14 perpendicular selection means A line selection means to control said vertical-drive means
15 to make the read-out means of each pixel line in said image pick-up field drive twice one
16 by one to desired signal are recording timing and signal read-out timing, It is prepared
17 corresponding to each pixel train in said image pick-up field, and two or more
18 perpendicular signal lines for transmitting perpendicularly the signal outputted,
19 respectively from each unit cell of the pixel line by which the sequential drive was
20 carried out with said vertical-drive means are provided. 1st means by which said line
21 selection means makes the read-out means of each of said pixel line drive to said signal
22 read-out timing with said vertical-drive means, It is characterized by providing 2nd at
23 least two means to make the read-out means of each of said pixel line drive to said signal
24 are recording timing with said vertical-drive means.

25 [0064] The 3rd solid state camera of this invention is set to said 2nd solid state camera.
26 Said image pick-up field At least three dummy pixel lines other than said two or more
27 pixel lines for signal read-out are provided further. Said line selection means It is
28 characterized by making one dummy pixel line in said dummy pixel line drive with said
29 1st means, and making other two dummy pixel lines in said dummy pixel line drive with
30 said 2nd two means.

31 [0065] It is characterized by the 4th solid state camera of this invention changing the
32 signal are recording timing within the period of 1 field period in said 2nd or 3rd solid
33 state camera in 1 field unit corresponding to the period of the signal read-out timing of
34 each pixel line in said line selection means.

35 [0066] In said 4th solid state camera, said 2nd at least two means changes relatively the
36 signal are recording timing to said signal read-out timing mutually, and makes said read-
37 out means drive, and the 5th solid state camera of this invention is characterized by
38 switching the control action of said vertical-drive means by said 2nd means by turns for
39 every field.

40 [0067] The 6th solid state camera of this invention is characterized by said line selection
41 means controlling said vertical-drive means to make the same substantially the electrical
42 potential difference of other wiring which adjoins said read line around said photo-
43 electric-conversion means also with the time of said two drives, in case the read-out
44 means of each pixel line in said image pick-up field is made to drive twice in said any 1st
45 thru/or 5th one solid state camera.

46 [0068] When the 7th solid state camera of this invention reads stored charge from the

1 optoelectric transducer of the unit cell arranged two-dimensional to the image pick-up
2 field on a semi-conductor substrate, In the solid state camera which performs electronic
3 shutter actuation to which the signal which was made to drive twice one by one to the
4 signal are recording timing and signal read-out timing of a request of wiring which
5 controls this read-out, and was read to said signal read-out timing is made to output
6 Wiring which controls said read-out is adjoined and it is characterized by making the
7 same substantially the electrical potential difference of other wiring which exists around
8 said optoelectric transducer to said signal are recording timing and signal read-out timing.
9 [0069] In the solid state camera with which, as for the 8th solid state camera of this
10 invention, the unit cell of 2 pixels / 1 unit has the image pick-up field which it comes to
11 arrange on a semi-conductor substrate two-dimensional In case stored charge is read from
12 the 2-pixel optoelectric transducer in the unit cell of said image pick-up field,
13 respectively, wiring which controls this read-out is adjoined and it is characterized by
14 making the same substantially the electrical potential difference of other wiring which
15 exists around said optoelectric transducer at the time of read-out of each pixel.
16 [0070]
17 [Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is
18 explained to a detail with reference to a drawing.
19 [0071] <Gestalt of the 1st operation> drawing 1 shows the equal circuit of the
20 magnification mold CMOS solid state camera of the gestalt of the 1st operation.
21 [0072] Although most is the same compared with the CMOS solid state camera of the
22 conventional example 2 which mentioned above the CMOS solid state camera of drawing
23 1 with reference to drawing 15 , perpendicular shift register 2a for read-out differs from
24 perpendicular shift register 15a for electronic shutters etc., and since others are the same,
25 they attach the same sign as the inside of drawing 15 .
26 [0073] The CMOS solid state camera of drawing 1 Namely, for example, the image pick-
27 up field 14 where the pixel cel 13 constituted as the conventional example 1 of drawing
28 12 showed has been arranged two-dimensional in the shape of a matrix (photo-electric-
29 conversion section), Two or more perpendicular signal lines VLIN formed in the
30 direction of a pixel train of said image pick-up field 14 Two or more perpendicular
31 selection lines 6 for read-out control for controlling to be formed in the pixel line writing
32 direction of said image pick-up field 14, and to read the photo-electric-conversion signal
33 of each pixel cel 13 to said two or more perpendicular signal lines VLIN per pixel line,
34 1st perpendicular selection-circuitry (perpendicular shift register for read-out) 2a for
35 carrying out a selection control in scan to the timing of read-out of said two or more
36 perpendicular selection lines 6 for read-out control, 2nd perpendicular selection-circuitry
37 (perpendicular shift register for electronic shutters) 15a for carrying out a selection
38 control in scan to the timing of signal are recording of said two or more perpendicular
39 selection lines 6 for read-out control, The vertical-drive circuit 16 which generates the
40 driving signal for driving alternatively said two or more perpendicular selection lines 6
41 for read-out control based on the output of said 1st perpendicular selection-circuitry 2a,
42 and the output of 2nd perpendicular selection-circuitry 15a (pulse selector), The level
43 selection transistor TH for choosing said perpendicular signal line VLIN, The level
44 selection circuitry 3 for carrying out the selection control of said level selection transistor
45 TH (level selection shift register), Output amplifying circuit AMP for outputting the
46 signal read to the level signal line HLIN and said level signal line HLIN for reading the

1 signal of said perpendicular signal line VLIN chosen with said level selection shift
2 register 3 It provides.

3 [0074] In addition, like the CMOS solid state camera of the conventional example 2 of
4 drawing 15 , although not illustrated especially here, it has a load transistor, a noise
5 canceller circuit, etc. as shown in drawing 12 around the image pick-up field 14.

6 [0075] and -- further -- (1) -- apart from the original pixel line, two dummy pixel lines
7 (the 1st dummy pixel line 141 and 2nd dummy pixel line 142) are added to said image
8 pick-up field 14. (2) Perpendicular shift register (1st perpendicular shift register) 2a for
9 said read-out has the shift number of stages of the original pixel line count +1 of the
10 image pick-up field 14, and perpendicular shift register (2nd perpendicular shift register)
11 15a for said electronic shutters also has the shift number of stages of the original pixel
12 line count +1 of the image pick-up field 14. (3) The vertical-drive circuit 16 is constituted
13 so that the last stage output signal of perpendicular shift register 2a for read-out is chosen,
14 said 1st dummy pixel line 141 may be supplied, the last stage output signal of
15 perpendicular shift register 15a for electronic shutters may be chosen and said 2nd
16 dummy pixel line 142 may be supplied.

17 [0076] Although it is the same configuration as an original pixel line, said two dummy
18 pixel lines 141 and 142 are added in order to act as a load, when chosen by the vertical-
19 drive circuit 16.

20 [0077] In the solid state camera of drawing 1 , shutter actuation which it is possible to
21 carry out the selection control of the same perpendicular selection line twice within 1
22 field period, and controls the signal storage time of a pixel (photodiode) by perpendicular
23 shift register 15a for electronic shutters and perpendicular shift register 2a for read-out
24 can be performed.

25 [0078] in this case, perpendicular shift register 15a for electronic shutters performs a shift
26 action based on the shift clock signal which controls the initiation timing of signal are
27 recording, carries out the selection control of the pixel line which each corresponds to a
28 shutter actuation period, and makes signal are recording of a pixel perform (read-out does
29 not perform) -- it controls like and the selection control of the 2nd dummy pixel line 142
30 carries out except a shutter actuation period (the period from after the end of selection of
31 a pixel line to next selection initiation).

32 [0079] Moreover, perpendicular shift register 2a for read-out performs a shift action
33 based on the shift clock signal which controls the initiation timing of signal read-out,
34 carries out the selection control of the pixel line which each corresponds to each level
35 period in the perpendicular effective scan period within a perpendicular period, and
36 carries out the selection control of the 1st dummy pixel line 141 to a vertical-retrace-line
37 period.

38 [0080] According to the solid state camera of the gestalt of implementation of the above
39 1st, namely, the vertical-drive circuit 16 Respectively corresponding to each output of
40 perpendicular shift register 2a for read-out, and perpendicular shift register 15a for
41 electronic shutters, are always carrying out the selection drive of the pixel line per (a total
42 of 2), and since the selection load is always equal Generating of the disk on the display
43 screen resulting from fluctuation of the read-out level by the size of a selection load can
44 be prevented.

45 [0081] <Gestalt of the 2nd operation> drawing 2 shows the equal circuit of the
46 magnification mold CMOS solid state camera of the gestalt of the 2nd operation.

1 [0082] As opposed to the CMOS solid state camera of the gestalt of the 1st operation
2 which mentioned above the CMOS solid state camera of drawing 2 with reference to
3 drawing 1 (1) The point that one more dummy pixel line (3rd dummy pixel line 143) is
4 added to said image pick-up field 14, (2) Perpendicular shift register 15b for one
5 electronic shutters which has the same shift number of stages as perpendicular shift
6 register 15a further for electronic shutters is added. The point which each of that stage
7 output switches per each stage output of perpendicular shift register 15a for said
8 electronic shutters, and field, is chosen, and is used by vertical-drive circuit (pulse
9 selector) 16a, (3) Vertical-drive circuit 16a Three perpendicular shift registers 2a and 15a,
10 Point and (4) vertical-drive circuits 16a which generates the driving signal for driving
11 alternatively said two or more perpendicular selection lines 6 for read-out control based
12 on the output of 15b The points which choose the last stage output signal of added
13 perpendicular shift register 15b for electronic shutters, and are supplied to said 3rd
14 dummy pixel line 143 differ a little, and since others are the same, they attach the same
15 sign as the inside of drawing 1 .
16 [0083] Drawing 3 is the timing chart showing signs that two perpendicular shift registers
17 15a and 15b for electronic shutters control electronic shutter actuation by turns per field,
18 in the solid state camera of drawing 2 .
19 [0084] In the solid state camera of drawing 2 , electronic shutter actuation is distributed
20 to two perpendicular shift registers 15a and 15b only for electronic shutters in the field
21 unit at alternation by making the shift action of two perpendicular shift registers 15a and
22 15b only for electronic shutters start by turns per field, and choosing each output by turns
23 per field so that it may understand from the timing chart shown in drawing 3 .
24 [0085] In this case, the selected perpendicular shift registers 15a and 15b only for
25 electronic shutters perform line selection ahead of perpendicular shift register 2a for read-
26 out, and it becomes possible by changing that timing to change the merits and demerits of
27 the time amount which accumulates a pixel signal.
28 [0086] Therefore, the same vertical lines can be chosen twice as 1 field period with the
29 perpendicular shift registers 15a and 15b for electronic shutters, and the perpendicular
30 shift register 2 for read-out, and good transformation child shutter actuation which
31 controls the signal storage time of a selection pixel can be performed.
32 [0087] Moreover, without while having already started the shift action, and being reset on
33 the way, before the shift action of the perpendicular shift registers 15a or 15b only for
34 electronic shutters arrives at the last stage even if an electronic shutter control signal is
35 inputted with a time interval shorter than a field period (before finishing no selection of
36 the pixel lines for read-out), sequential selection is made to the last pixel line, and the
37 signal storage time of a selection pixel is controlled.
38 [0088] And the period from after the end of selection of the last line of the pixel line for
39 read-out to selection initiation [in / one after another / the field period of a time] of the
40 pixel line for read-out of the 1st line carries out the selection control of the 2nd dummy
41 pixel line 142 or the 3rd dummy pixel line 143.
42 [0089] Moreover, perpendicular shift register 2a for read-out carries out the selection
43 control of the pixel line which each corresponds to each level period within a
44 perpendicular effective scan period, and carries out the selection control of the 1st
45 dummy pixel line 141 to a vertical-retrace-line period.
46 [0090] That is, each perpendicular shift registers 2a, 15a, and 15b continue choosing a

dummy pixel line, even after choosing the pixel line for all read-out, respectively, and they stand by the selection initiation in a next field period.

[0091] That is, according to the solid state camera of the gestalt of implementation of the above 2nd, it becomes possible in a field unit to change the signal storage time to two perpendicular shift registers only for electronic shutters between the fields by distributing electronic shutter actuation at alternation.

[0092] In this case, it becomes possible to realize electronic shutter ability to which the signal storage time is continuously changed per field, while the scan time of read-out has been fixed. In addition, in the same field, every selection pixel line of the signal storage time is the same.

[0093] Thus, when changing the signal storage time and making good transformation child shutter actuation perform, it can prevent that the difference of the signal storage time arises to pixel spacing according to the merits and demerits of the signal storage time, and generating of image noises, such as a lateral stripe in the display screen of an output signal, can be prevented.

[0094] Moreover, vertical-drive circuit 16a is always carrying out the selection drive of the pixel line per (a total of 3) respectively corresponding to each output of perpendicular shift register 2a for read-out, and the perpendicular shift registers 15a and 15b for two electronic shutters, and since the selection load is always equal, it can prevent generating of the disk on the display screen resulting from fluctuation of the read-out level by the size of a selection load.

[0095] In addition, the solid state camera shown in drawing 1 and drawing 2 is applicable not only to the solid state camera of the CMOS mold equipped with the readout circuitry which a pixel signal can read for every pixel but the solid state camera of the CCD (charge coupled devices) mold which reads in a level signal-line unit.

[0096] <Gestalt of the 3rd operation> drawing 4 shows the equal circuit of the magnification mold CMOS solid state camera of the gestalt of the 3rd operation.

[0097] When the CMOS solid state camera of drawing 4 changes the signal storage time automatically according to the output level of a photo sensor as opposed to the CMOS solid state camera of the conventional example 1 mentioned above with reference to drawing 12, the device is made so that it may become possible to change continuously the good transformation child shutter actuation to which light-receiving time amount is changed equivalent per field.

[0098] Namely, although most is the same compared with the CMOS solid state camera of the conventional example 1 which mentioned above the CMOS solid state camera of drawing 4 with reference to drawing 12 (1) The point that two perpendicular shift registers 21 and 22 for electronic shutters are added independently [the perpendicular shift register 2 for read-out], (3) The point that the register change-over control circuit (SEL) 23 for switching actuation (output actuation of the control pulse of the signal storage time) of two perpendicular shift registers 21 and 22 for electronic shutters by turns per field, and controlling it is added, (4) The configurations of timing generating circuit 10a and the pulse selector circuit 24 differ, and since others are the same, they attach the same sign as the inside of drawing 12.

[0099] That is, in drawing 4, four transistors Ta, Tb, Tc, and Td and the unit cell of 1 pixel (1 pixel) / 1 unit which consists of one photodiode PD are arranged in the shape of [which is two dimensions] a matrix, and are formed in the cel field (image pick-up field).

1 In this case, the photodiode PD with which, as for each unit cell, touch-down potential is
2 given to an anode side The read-out transistor Td by which the end side is connected to
3 the cathode side of Photodiode PD (shutter gate transistor). The magnification transistor
4 Tb by which the gate is connected to the other end side of the read-out transistor Td The
5 reset transistor Tc by which the end side is connected to the gate of the perpendicular
6 selection transistor (line selection transistor) Ta and the magnification transistor Tb
7 where the end side is connected to the end side of the magnification transistor Tb is
8 provided.

9 [0100] And two or more read lines 4 connected to said cel field corresponding to each,
10 pixel line common to the gate of each read-out transistor Td of the unit cell of the same
11 line, the perpendicular selection line 6 connected common to the gate of each
12 perpendicular selection transistor Ta of the unit cell of the same line, and the reset line 7
13 connected common to the gate of each reset transistor Tc of the unit cell of the same line
14 are formed.

15 [0101] Moreover, corresponding to each pixel train, the power-source line 9 connected
16 common to the other end [of each reset transistor Tc of the unit cell of the same train as
17 the perpendicular signal line VLIN connected common to the other end side of each
18 magnification transistor Tb of the unit cell of the same train] and other end side of each
19 perpendicular selection transistor Ta is formed in said cel field.

20 [0102] Furthermore, in the exterior by the side of the end of a cel field, two or more load
21 transistors TL connected, respectively between one one end each of said perpendicular
22 signal line VLIN and a touch-down node are arranged horizontally.

23 [0103] Moreover, in the exterior by the side of the other end of a cel field, two or more
24 noise canceller circuits which consisted of two transistors TSH and TCLP and two
25 capacitors Cc and Ct are arranged horizontally.

26 [0104] And two or more level selection transistors TH connected to each other end side
27 of said perpendicular signal line VLIN through each above-mentioned noise canceller
28 circuit are arranged horizontally.

29 [0105] The level signal line HLIN is connected to each other end of the above-mentioned
30 level selection transistor TH in common, and they are a level reset transistor (not shown)
31 and the output amplifying circuit AMP in this level signal line HLIN. It connects.

32 [0106] In addition, the transistor TSH for sample hold by which, as for said each noise
33 canceller circuit, the end side was connected to the other end side of the perpendicular
34 signal line VLIN Coupling-capacitor Cc by which the end side was connected to the other
35 end side of the transistor TSH for these sample hold, The capacitor Ct for charge storages
36 connected between touch-down nodes the other end side of this coupling-capacitor Cc, It
37 is constituted by the transistor TCLP for a potential clamp connected to the connection
38 node of said capacitors Cc and Ct, and the end side of said level selection transistor TH is
39 connected to the connection node of said capacitors Cc and Ct.

40 [0107] furthermore, in the exterior of a cel field The selection control of the output pulse
41 of the perpendicular shift register 2 for read-out for carrying out the selection control of
42 two or more perpendicular selection lines 6 of a cel field in scan, two perpendicular shift
43 registers 21 and (ES2) 22 for electronic shutters (ES1), and the three above-mentioned
44 perpendicular shift registers 2, 21, and 22 is carried out. The perpendicular selection line
45 6 of each line of a cel field Actuation (output actuation of the control pulse of the signal
46 storage time) of the level shift register 3 for driving the pulse selector 24 for driving in

1 scan, and said two or more level selection transistors TH in scan, and said perpendicular
 2 shift registers 21 and 22 for two electronic shutters The register change-over control
 3 circuit 23 for switching by turns per field and controlling, timing generating circuit which
 4 generates various kinds of timing signals 10a, The bias generating circuit 11 for
 5 generating predetermined bias potential at the end of the transistor TCLP for the potential
 6 clamp of said noise canceller circuit etc. is arranged, respectively.
 7 [0108] Timing signal phiVR of a field period, timing signal phiES for storage-time
 8 control by which an adjustable setup is carried out with a field period, pulse signal phiHP
 9 corresponding to a horizontal blanking interval, and clock pulse signal phiCK input said
 10 timing generating circuit 10a.
 11 [0109] And timing signal phiVRR for carrying out buffer plastic surgery, reading said
 12 timing signal phiVR input, and supplying the perpendicular shift register of business is
 13 generated, and timing signal phiHPV for carrying out buffer plastic surgery, reading said
 14 pulse signal phiHP input, and supplying the perpendicular shift register of business and
 15 two perpendicular shift registers 21 and 22 for electronic shutters is generated.
 16 [0110] Moreover, timing signal phiROREAD for supplying said pulse selector 24,
 17 phiESREAD, phiRESET, and phiADRES are generated, and pulse signal phiCLP for
 18 supplying said noise canceller circuit and phiSH are generated. Moreover, pulse signal
 19 phiH for supplying the level shift register 3 is generated.
 20 [0111] Moreover, based on timing signal phiVR of a field period, pulse signal phiFI for
 21 field change-over control is generated, and said register change-over control circuit 23 is
 22 supplied with timing signal phiESR for signal storage-time control.
 23 [0112] Said register change-over control circuit 23 switches the supply place of timing
 24 signal phiESR for storage-time control by turns for every field unit based on the pulse
 25 signal phiFI input for field change-over control. In this case, the timing signal for signal
 26 storage-time control which supplies the timing signal for signal storage-time control
 27 supplied to the perpendicular shift register 21 for said electronic shutters to phiESR1 and
 28 the perpendicular shift register 22 for said electronic shutters is expressed with phiESR2.
 29 [0113] Drawing 5 is the circuit diagram showing an example of the pulse selector 24 in
 30 drawing 4 .
 31 [0114] While each output-signal ES1n of the output signal ROn of the perpendicular shift
 32 register for read-out and two perpendicular shift registers 21 and 22 for electronic
 33 shutters and ES2n input the pulse selector shown in drawing 5 Timing signal
 34 phiROREAD supplied from said timing generating circuit 10a, phiESREAD, phiRESET,
 35 and phiADRES input, logic processing of these input signals is performed and various
 36 kinds of driving signal phiREADn(s), phiRESET, and phiADRESn are outputted, and it
 37 is constituted by the logic gate so that a cel field may be supplied.
 38 [0115] That is, when the output signal ROn of the perpendicular shift register for read-out
 39 is an active state, timing signal phiROREAD is chosen and read and it outputs as line
 40 driving signal phiREADn, and when each output signal ES1n of two perpendicular shift
 41 registers 21 and 22 for electronic shutters or ES2n is an active state, timing signal
 42 phiESREAD is chosen and read and it outputs as line driving signal phiREADn.
 43 [0116] Moreover, when any one of each output-signal ES1n of the output signal ROn of
 44 the perpendicular shift register for read-out and two perpendicular shift registers 21 and
 45 22 for electronic shutters and the ES2n is an active state, timing signal phiRESET is
 46 chosen and it outputs as reset line driving signal phiRESETn.

1 [0117] Moreover, when the output signal ROn of the perpendicular shift register for read-
2 out is an active state, timing signal phiADRES is chosen and it outputs as perpendicular
3 selection line driving signal phiADRESn.

4 [0118] Drawing 6 is the timing wave form chart showing the example of timing
5 generating circuit 10a in drawing 4 , three perpendicular shift registers 2, 21, and 22, and
6 the pulse selector 24 of operation, in order to explain the good transformation child
7 shutter actuation with possible making it change continuously in the field unit in the solid
8 state camera of drawing 4 .

9 [0119] Here, the case where the solid state camera of drawing 4 is used by 1 field = 1 /
10 30Hz (image of 30 frames per second which make the 1 field one frame) image pick-up
11 system is shown.

12 [0120] The timing signal input for storage-time control by which an adjustable setup of
13 the timing signal input of a field period and the phiES is carried out for phiVR with a
14 field period in drawing 6 , The timing signal of a field period with which phiVRR is
15 supplied to the perpendicular shift register for read-out, The pulse signal for field change-
16 over control in phiFI, the timing signal for storage-time control with which phiESR1 is
17 supplied to the perpendicular shift register 21 for one electronic shutters every other field,
18 The timing signal for storage-time control with which phiESR2 is supplied to the
19 perpendicular shift register 22 for the electronic shutters of another side at intervals of 1
20 field, R0 (i) is the output of the perpendicular shift register R0 for read-out, and ES1 (i).
21 The output of the perpendicular shift register 21 for one electronic shutters, and ES2 (i) It
22 is the output of the perpendicular shift register 22 for the electronic shutters of another
23 side.

24 [0121] Drawing 7 is the timing wave form chart showing an example of the electronic
25 shutter actuation within 1 field period in drawing 6 .

26 [0122] In drawing 7 , the perpendicular shift register 21 for electronic shutters in ESn or
27 the n-th step of output signal of 22, and ROn are the n-th step of output signals of the
28 perpendicular shift register 2 for read-out.

29 [0123] tHES shows 1 level period when the perpendicular shift register 21 for electronic
30 shutters or the n-th step of output signal ESn of 22 will be in an active state ("H" level).

31 [0124] tHRO shows 1 level period when the n-th step of output signal ROn of the
32 perpendicular shift register 2 for read-out will be in an active state ("H" level).

33 [0125] HBLK is a control pulse signal for dividing 1 level period into a horizontal
34 blanking interval and a horizontal effective scan period.

35 [0126] phiCLP and phiSH are pulse signals supplied to a noise canceller circuit, and are
36 generated for every horizontal blanking interval, respectively.

37 [0127] phiH is a pulse signal supplied to the level selection transistor TH, and it is
38 generated so that the level selection transistor TH horizontally arranged within a level
39 effective-scanning-lines period may be turned on [sequential].

40 [0128] Although phiADRES, phiRESET, and phiREAD are pulse signals supplied to a
41 selection pixel line from said pulse selector 24 and phiRESET of them and phiREAD are
42 activated within a horizontal blanking interval in the case of signal are recording
43 actuation and signal read-out actuation, respectively, phiADRES is not generated in the
44 case of signal are recording actuation, but is activated within a horizontal blanking
45 interval in the case of signal read-out actuation.

46 [0129] In this case, the above-mentioned pulse signal phiADRES is generated so that the

1 selection control of the perpendicular selection line 6 of the same line may be carried out
2 twice within the horizontal blanking interval in the case of signal read-out actuation and it
3 may be in an active state twice intermittently for a reason which is mentioned later.

4 [0130] Next, actuation of the solid state camera of drawing 4 is explained, referring to
5 drawing 6 and drawing 7.

6 [0131] Since actuation of the solid state camera of drawing 4 is fundamentally the same
7 compared with actuation (drawing 13) of the solid state camera (drawing 12) of the
8 conventional example 1 mentioned above, explanation of the same actuation is omitted,
9 and mainly different actuation is explained hereafter.

10 [0132] That is, in case the solid state camera of drawing 4 performs electronic shutter
11 actuation, it is distributed to two perpendicular shift registers 21 and 22 only for [
12 electronic shutter actuation / unit / field / alternation] electronic shutters by making the
13 shift action of two perpendicular shift registers 21 and 22 for electronic shutters start by
14 turns per field by the register change-over control circuit 23, and choosing each output by
15 turns per field.

16 [0133] As shown at the field periods t_{Fa} and t_{Fb} in drawing 6, even if timing signal
17 ϕ_{iES} for signal storage-time control is inputted with a time interval shorter than a field
18 period by this, it enables the perpendicular shift registers 21 and 22 only for electronic
19 shutters to operate to coincidence.

20 [0134] In this case, it becomes possible to make sequential selection to the last of the
21 pixel line for read-out, and to control the signal storage time of a selection pixel, without
22 being reset on the way, before the perpendicular shift register 21 only for electronic
23 shutters or the shift action of 22 reads and while having already started the shift action by
24 timing signal ϕ_{iESR1} or ϕ_{iESR2} generated first finishes no selection control of the
25 pixel lines of business.

26 [0135] If it puts in another way, it will become possible to realize electronic shutter
27 ability (continuation electronic shutter actuation) to which the signal storage time is
28 continuously changed per field, while the scan time of read-out has been fixed. In
29 addition, in the same field, every selection pixel line of the signal storage time is the
30 same.

31 [0136] Moreover, as shown in drawing 7, pulse signal ϕ_{iRESET} and ϕ_{iREAD} are
32 supplied to the pixel line of the n-th line which carried out the selection control to said
33 level period t_{HES} with the output signal ES_n of shift [the n-th step of] stage of the
34 perpendicular shift register for electronic shutters, and the signal charge of a photodiode
35 is made into zero by reading the signal charge which was being accumulated before it
36 with the photodiode PD of this pixel line of the n-th line to the gate of the transistor for
37 magnification.

38 [0137] In this case, pulse signal ϕ_{iADRES} continues being "L", and since the transistor
39 for perpendicular selection is still OFF, the signal charge read to the gate of said
40 transistor for magnification is not outputted to the perpendicular signal line VLIN.

41 [0138] Then, in the case of the signal read-out actuation from said pixel line, after
42 ϕ_{iRESET} is activated temporarily at the horizontal blanking interval in said level period
43 t_{HRO} , ϕ_{iADRES} is activated and ϕ_{iREAD} is activated further temporarily.

44 [0139] In this case, when the aforementioned ϕ_{iREAD} is an active state ("H" level), so
45 that the diving of the noise under the effect of capacity coupling between a photodiode
46 and its circumference wiring (ϕ_{iADRES} wiring later mentioned in this example) may

1 not occur phiADRES pulse is temporarily made into a non-active state ("L" level) so that
2 it may be in the same condition as the time of signal are recording actuation, and this
3 phiADRES is activating the aforementioned phiREAD temporarily within the period of a
4 non-active state.

5 [0140] First, if the actuation at the time of signal read-out within the horizontal blanking
6 interval in said such level period tHRO is explained in detail, after resetting the gate
7 electrode of the magnification transistor Tb to a reference potential by phiRESET,
8 phiADRES will be made into an active state (the 1st time), the perpendicular selection
9 transistor Ta of said pixel line of the n-th line will be made into an ON state, pulse signal
10 phiCLP supplied to a noise canceller circuit within this activity period will be activated,
11 and black level will be clamped.

12 [0141] And when phiADRES activates phiREAD within the period of a non-active state,
13 the signal charge which was being accumulated before it with said photodiode PD is read
14 to the gate of the magnification transistor Tb.

15 [0142] And phiADRES is again made into an active state (the 2nd time), the
16 perpendicular selection transistor Ta of said pixel line of the n-th line is again made into
17 an ON state, and the signal charge read to the gate of said magnification transistor Tb is
18 outputted to the perpendicular signal line VLIN.

19 [0143] By the above actuation, from the termination point in time of the active state ("H"
20 level) of read line driving signal phiREAD in said level period tHES to the activation
21 time of read line driving signal phiREAD in said level period tHRO serves as the signal
22 storage time.

23 [0144] Drawing 8 (a) is the top view taking out and showing a part of unit cell of an
24 image pick-up field, in order to explain the diving of said noise.

25 [0145] Drawing 8 (b) is a sectional view which meets the a-a' line of this drawing (a).
26 [0146] Drawing 8 (c) and (d) correspond, respectively, and when phiADRES in this
27 drawing (a) is "L" level and it is /"H" level, they show the potential potential in the
28 substrate in the case of phiREAD being activated and reading a signal charge. Here, the
29 case where power-source potential is 3.3V is shown.

30 [0147] the P type with which 81 was formed in the surface section of a silicon substrate
31 in drawing 8 (a) and (b) -- a well -- a field and 82 are the component isolation regions
32 (for example, LOCOS field) alternatively formed in the substrate surface section. n mold
33 field (detection node DN) used as n mold field which serves as the cathode field of a
34 photodiode and the source field of the read-out transistor Td, and the drain field of the
35 read-out transistor Td is alternatively formed in the component field of the substrate
36 surface section.

37 [0148] On the channel field of the above-mentioned read-out transistor Td, the gate
38 electrode (a part of read line 4) which consists of polish recon wiring through the
39 insulated-gate film is formed, and the perpendicular selection line 5 and the reset line 7
40 which consist of polish recon wiring on the component isolation region 82 near the n
41 mold field of Photodiode PD are formed in abbreviation parallel.

42 [0149] Since phiREAD is activated and a signal charge is read on the occasion of read-
43 out actuation of the gestalt of this operation when phiADRES wiring contiguous to
44 Photodiode PD is "L" level, as shown in drawing 8 (c), the potential potential in the
45 substrate under Photodiode PD with the joint capacity calcium which exists between
46 Photodiode PD and phiADRES wiring - Only VCa is reduced and the stored charge QCa

1 of Photodiode PD is read.
2 [0150] On the other hand, if phiREAD is activated and a signal charge is read when
3 phiADRES wiring contiguous to Photodiode PD is "H" level, as shown in drawing 8 (d)
4 By that from which the potential potential in the substrate under Photodiode PD can pull
5 up only + VCa with the joint capacity calcium which exists between Photodiode PD and
6 phiADRES wiring (it becomes the diving of a noise) When a part for the stored charge
7 QCa of Photodiode PD is no longer read and the output signal of a solid state camera is
8 displayed on the screen of an image display device, a black signal is crushed and it
9 becomes an unsightly image.
10 [0151] Also in the solid state camera of the gestalt of implementation of the above 3rd in
11 addition, like the solid state camera of the gestalt of said 2nd operation Add the 3rd
12 dummy pixel line and the shift number of stages of the (2) 3 piece perpendicular selection
13 circuitries 2, 21, and 22 is made into the number of stages of the pixel line count +1 for
14 an original image pick-up. (1) -- said image pick-up field -- the 1- (3) When the driving
15 signal for driving alternatively two or more horizontal control-line groups (4, 6, 7) based
16 on the output of the perpendicular selection circuitries 2, 21, and 22 is generated by the
17 pulse selector 24, The activation period of the last stage output signal of the
18 perpendicular selection circuitry 2 chooses and drives the 1st dummy pixel line. The
19 activation period of the last stage output signal of the 2nd perpendicular selection
20 circuitry 21 chooses and drives the 2nd dummy pixel line, and the activation period of the
21 last stage output signal of the 3rd perpendicular selection circuitry 22 may be constituted
22 so that the 3rd dummy pixel line may be chosen and driven.
23 [0152] Such a configuration enables it for the pulse selector 24 to always come to carry
24 out the selection drive of the pixel line per (a total of 3) respectively corresponding to
25 each output of the perpendicular shift register 2 for read-out, and two perpendicular shift
26 registers 21 and 22 for electronic shutters, and to prevent generating of the disk on the
27 display screen resulting from fluctuation of the read-out level by the size of a selection
28 load, since the selection load is always equal.
29 [0153] In addition, although the gestalt of said 3rd operation explained the case where
30 phiADRES wiring existed as circumference wiring which the problem of black crushing
31 by capacity coupling with Photodiode PD produces Since there is a possibility that the
32 problem of crushing (black crushing) of the black signal by capacity coupling of these
33 wiring and Photodiodes PD may arise also when phiRESET wiring or other wiring exist
34 as the above-mentioned circumference wiring What is necessary is just to control level
35 like phiADRES wiring in the gestalt of said 3rd operation also about these wiring.
36 [0154] namely, as applied voltage of circumference wiring of photodiodes PD other than
37 read-out gate wiring which adjoins Photodiode PD as described above By impressing the
38 same electrical potential difference as the activation period of signal read-out pulse
39 phiREAD at the time of signal read-out actuation, and the activation period of read-out
40 pulse phiREAD at the time of electronic shutter actuation it can come out and perform
41 controlling so that an excessive charge is not read from Photodiode PD by capacity
42 coupling of Photodiode PD and circumference wiring, and a reconstruction image
43 without the so-called black crushing is acquired.
44 [0155] In addition, this invention is applicable also to the solid state camera which has
45 the array of the unit cell of 2 pixels / 1 unit which is stated to the gestalt of the following
46 operation [4th] according to the gestalt of said the operation of each.

1 [0156] <Gestalt of the 4th operation> drawing 9 shows the equal circuit of the unit cell of
2 2 pixels / 1 unit in the magnification mold CMOS solid state camera of the gestalt of the
3 4th operation. Since this CMOS solid state camera can be constituted like the gestalt of
4 each operation mentioned above except the configuration of a unit cell, it mainly explains
5 the configuration of the unit cell of 2 pixels / 1 unit hereafter.

6 [0157] The unit cell 30 shown in drawing 9 has two photodiodes 31a and 31b, touch-
7 down potential is given to each anode side, each cathode side corresponds, respectively,
8 and reads these two photodiodes 31a and 31b, and is connected common to the gate of
9 one magnification transistor 33 through Transistors (shutter gate transistor) 32a and 32b.
10 The read lines 4a and 4b are connected to each gate of the two above-mentioned read-out
11 transistors 32a and 32b, respectively.

12 [0158] An end side is connected to the perpendicular signal line VLIN, the other end side
13 is connected to the power-source line 9 through the perpendicular selection transistor 34
14 (that is, said magnification transistor 33 source follower connection), and, as for said
15 magnification transistor 33, the perpendicular selection line (address line) 6 is connected
16 to the gate of the above-mentioned perpendicular selection transistor 34.

17 [0159] Furthermore, one reset transistor 35 is connected between the gate of said
18 magnification transistor 33, and the power-source line 9, and the reset line 7 is connected
19 to the gate of this reset transistor 35.

20 [0160] The unit cell of 2 pixels / 1 unit of the above-mentioned configuration is arranged
21 in the shape of [2-dimensional] a matrix to an image pick-up field. And said two read
22 lines (1st read line 4a and 2nd read line 4b), perpendicular selection lines (address line) 6,
23 and reset lines 7 are formed horizontally on an image pick-up field, and said
24 perpendicular signal line VLIN and the power-source line 9 are perpendicularly formed
25 on the image pick-up field.

26 [0161] Drawing 10 (a) shows an example of the flat-surface pattern of the unit cell of 2
27 pixels / 1 unit of drawing 9 , and shows drawing 10 (b) for the cross-section structure of
28 meeting the B-B line, roughly.

29 [0162] In drawing 10 (a) and (b), 90 is an N type silicon substrate and P wells 91 are
30 formed in the surface section. In the surface section of these P wells 91 The N type
31 impurity range 931, the cathode field of photodiode 31b of another side used as the
32 component isolation region (for example, LOCOS field) 92, the cathode field of one
33 photodiode 31a, and the source field of one read-out transistor 32a And the N type
34 impurity range 932 used as the source field of read-out transistor 32b of another side and
35 the SDG field (only the N type impurity range 94 which reads to drawing and serves as a
36 common drain of Transistors 32a and 32b is shown) of an NMOS transistor are formed
37 alternatively.

38 [0163] And silicon oxide (gate dielectric film) 95 is formed on a substrate front face, and
39 the field ion in plastic field 96 is formed in the bottom of the base of said LOCOS field
40 92.

41 [0164] Polish recon gate wiring whose 97 contains the gate electrode of the magnification
42 transistor 33 in a part, the N type impurity range where 98 becomes the drain field of the
43 magnification transistor 33 and the source field of the perpendicular selection transistor
44 34, and 99 are the N type impurity ranges used as the source field of the reset transistor
45 35.

46 [0165] 100 is wiring which connects the source field 99 of the reset transistor 35, the gate

1 wiring 97 of the magnification transistor 33, and the common drain field of two read-out
2 transistors 32a and 32b.

3 [0166] Polish recon gate wiring whose read line 4a contains the gate electrode of read-out
4 transistor 32a in a part, and read line 4b consist of polish recon gate wiring which
5 contains the gate electrode of read-out transistor 32b in a part.

6 [0167] Polish recon gate wiring with which the perpendicular selection line (address line)
7 6 contains the gate electrode of the perpendicular selection transistor 34 in a part, and the
8 reset line 7 consist of polish recon gate wiring which contains the gate electrode of the
9 reset transistor 35 in a part.

10 [0168] 33a is the contact section of the source field of said magnification transistor 33,
11 and the perpendicular signal line VLIN, and 34a is the contact section of the drain field of
12 the above-mentioned perpendicular selection transistor 34, and the power-source line 9.
13 For 97a, the contact section of the gate wiring 97 of the magnification transistor 33 and
14 wiring 100 and 99a are [the contact section of the drain field of the reset transistor 35
15 and the power-source line 9 and 100a of the contact section of the source field 99 of the
16 reset transistor 35 and wiring 100 and 99b] the contact sections of the above-mentioned
17 wiring 100 and the common drain field of two read-out transistors 32a and 32b.

18 [0169] Although the basic actuation which actuation of the unit cell of 2 pixels / 1 unit of
19 the above-mentioned configuration operates five transistors in predetermined sequence
20 compared with actuation of the unit cell of said 1 pixel / 1 unit, and reads a signal charge
21 from a photodiode is the same, the points which read a signal charge to timing which is
22 different from two photodiodes 31a and 31b differ. That is, it is supposed that the read
23 signal of "H" level is given to 1st read line 4a when reading a signal charge from one
24 photodiode 31a, and the read signal of "L" level has been given to 2nd read line 4b.
25 Suppose that the read signal of "H" level is given to 2nd read line 4b when reading a
26 signal charge from photodiode 31b of another side, and the read signal of "L" level has
27 been given to 1st read line 4a.

28 [0170] In the CMOS solid state camera which has <the gestalt of the 5th operation>, and
29 the array of a unit cell of 2 pixels / 1 unit which was described above in time By driving
30 an address-line driving signal twice intermittently, as it described above, when not giving
31 electronic shutter ability which was described above and reading a signal charge to
32 timing which is different from two photodiodes 31a and 31b It becomes possible to
33 prevent the problem of generating of the disk on the display screen at the time of
34 displaying an output signal on the screen of an image display device.

35 [0171] Drawing 11 is the timing wave form chart showing an example of signal read-out
36 actuation of a part of 1 field period in the CMOS solid state camera of the gestalt of the
37 5th operation.

38 [0172] In drawing 11 , although phiRESET, phiADRES, phiREAD1, or phiREAD2 is a
39 pulse signal supplied to a selection pixel line from a pulse selector and it activates within
40 a horizontal blanking interval in the case of signal read-out actuation, respectively,
41 phiREAD1 and phiREAD2 are supplied within a different horizontal blanking interval.

42 [0173] Here rather than the distance of the 1st read line 4a and the address line 6 to which
43 phiREAD1 is supplied Since the distance of the 2nd read line 4b and the address line 6 to
44 which phiREAD2 is supplied is short and the joint capacity of 2nd read line 4b and the
45 address line 6 is larger than the joint capacity of 1st read line 4a and the address line 6 It
46 originates in the effects to the signal charge read from two photodiodes 31a and 31b,

1 respectively differing, and there is a possibility that the disk on the display screen at the
2 time of displaying an output signal on the screen of an image display device may occur.
3 [0174] However, phiADRES so that the selection control of the address line 6 of the
4 same line may be carried out twice within the horizontal blanking interval in the case of
5 signal read-out actuation Since phiADRES has "L" level, respectively when it is
6 generated so that it may be in an active state twice intermittently, and reading a signal
7 charge from two photodiodes 31a and 31b, respectively The problem of generating of the
8 disk on the display screen which the effect of [at the time of the above-mentioned signal-
9 charge read-out] becomes almost equal, and was described above can be prevented.
10 [0175] Moreover, this invention is applicable not only to the solid state camera of the
11 type of the gestalt of each above-mentioned implementation but the solid state camera of
12 the laminating mold which carried out the laminating of the photo-electric-conversion
13 section.
14 [0176]
15 [Effect of the Invention] According to the solid state camera of each claim subordinate to
16 claim 1 and it, when making electronic shutter actuation perform, fluctuation of the load
17 of the perpendicular shift register for read-out and the perpendicular shift register for
18 electronic shutters can be prevented, the image noise of the lateral stripe generated in the
19 display screen of an output signal can be controlled, and the clear high image of S/N can
20 be obtained.
21 [0177] According to the solid state camera of each claim subordinate to claim 3 and it,
22 the good transformation child shutter actuation (continuation electronic shutter actuation)
23 to which the signal storage time is changed per field is realizable by distributing
24 electronic shutter actuation to the shift register only for [of two pieces] electronic
25 shutters by turns per field. In this case, it can prevent that the difference of the signal
26 storage time arises to pixel spacing according to the merits and demerits of the signal
27 storage time, and generating of image noises, such as a lateral stripe in the display screen
28 of an output signal, can be prevented.
29 [0178] according to especially the solid state camera of claim 4, continuation electronic
30 shutter actuation is realizable like the solid state camera of claim 3 -- both Two dummy
31 pixel lines are prepared corresponding to the perpendicular shift register only for [of two
32 pieces] electronic shutters. By always carrying out the selection drive of the three pixel
33 lines by which a selection control is carried out with the shift register for read-out, and
34 the shift register only for [of two pieces] electronic shutters, fluctuation of the load
35 accompanying pixel line selection is lost, and generating of the lateral stripe on the
36 display screen can be prevented.
37 [0179] According to the solid state camera of each claim subordinate to claim 10 and it
38 Electronic shutter actuation is realizable, and also the applied voltage of circumference
39 wiring of those other than the read-out gate contiguous to a photodiode It considers as the
40 same electrical potential difference in both the activation period of the read-out pulse
41 signal at the time of signal read-out actuation, and the activation period of the read-out
42 pulse signal at the time of electronic shutter actuation. A reconstruction image without
43 black crushing is acquired by controlling read-out of the excessive charge from the
44 photodiode by capacity coupling with wiring.
45 [0180] When reading stored charge from the 2-pixel optoelectric transducer in the unit
46 cell of 2 pixels / 1 unit of an image pick-up field, respectively according to the solid state

1 camera of the claim subordinate to claim 12 and it, Since the electrical potential
2 difference of other wiring which adjoins wiring which controls this read-out and exists
3 around said optoelectric transducer is substantially made the same at the time of read-out
4 of each pixel When reading a signal charge from a 2-pixel optoelectric transducer,
5 respectively, the effect which the electrical potential difference of other wiring does
6 becomes almost equal, and can prevent the problem of generating of the disk on the
7 display screen.

8 9 DESCRIPTION OF DRAWINGS

10 [Brief Description of the Drawings]

11 [Drawing 1] Drawing showing the equal circuit of the CMOS solid state camera of the
12 gestalt of operation of the 1st of this invention.

13 [Drawing 2] Drawing showing the equal circuit of the CMOS solid state camera of the
14 gestalt of operation of the 2nd of this invention.

15 [Drawing 3] The timing chart showing signs that two perpendicular shift registers for
16 electronic shutters control electronic shutter actuation by turns per field in the solid state
17 camera of drawing 2 .

18 [Drawing 4] Drawing showing the equal circuit of the CMOS solid state camera of the
19 gestalt of operation of the 3rd of this invention.

20 [Drawing 5] The circuit diagram showing an example of the pulse selector in drawing 4 .

21 [Drawing 6] the timing generating circuit in drawing 4 , and perpendicular shift register [
22 of ** a 1st] - the timing wave form chart showing the 3rd perpendicular shift register and
23 the example of a pulse selector of operation.

24 [Drawing 7] It is the timing wave form chart showing an example of the electronic
25 shutter actuation within 1 field period in drawing 6 .

26 [Drawing 8] Drawing showing the potential potential in the top view showing a part of
27 unit cell of an image pick-up field in order to explain the actuation which controls the
28 diving of a noise in the electronic shutter actuation shown in drawing 7 , a sectional view,
29 and a substrate.

30 [Drawing 9] Drawing showing the equal circuit of the unit cell of 2 pixels / 1 unit in the
31 magnification mold CMOS solid state camera of the gestalt of operation of the 4th of this
32 invention.

33 [Drawing 10] Drawing showing roughly an example of the flat-surface pattern of the unit
34 cell of 2 pixels / 1 unit of drawing 9 , and an example of the cross-section structure.

35 [Drawing 11] The timing wave form chart showing an example of the signal read-out
36 actuation within 1 field period in the CMOS solid state camera of the gestalt of operation
37 of the 5th of this invention.

38 [Drawing 12] Drawing showing the equal circuit of the CMOS solid state camera of the
39 conventional example 1.

40 [Drawing 13] The timing wave form chart showing the example of the CMOS solid state
41 camera of drawing 12 of operation.

42 [Drawing 14] The timing wave form chart showing the example of the timing generating
43 circuit in drawing 13 , a perpendicular shift register, and a pulse selector of operation.

44 [Drawing 15] Drawing showing the equal circuit of the CMOS solid state camera of the
45 conventional example 2.

1 [Drawing 16] Drawing showing an example of the line selection timing of two
2 perpendicular shift registers in drawing 15 .

3 [Drawing 17] in order to change the signal storage time in the solid state camera of
4 drawing 15 -- the perpendicular shift register for electronic shutters -- reading -- business
5 -- the timing chart shown in order to explain the trouble in the case of changing the merits
6 and demerits of the time amount which the timing which performs line selection ahead of
7 a perpendicular shift register is changed, and accumulates a pixel signal.

8 [Description of Notations]

9 2 -- Perpendicular shift register for read-out,

10 3 -- Level shift register,

11 4 -- Read line,

12 6 -- Perpendicular selection line,

13 7 -- Reset line,

14 9 -- Power-source line,

15 10a -- Timing generating circuit,

16 21 22 -- Perpendicular shift register for electronic shutters,

17 23 -- Change-over control circuit,

18 24 -- Vertical-drive circuit (pulse selector),

19 PD -- Photodiode,

20 Ta -- Perpendicular selection transistor (line selection transistor),

21 Tb -- Magnification transistor,

22 Tc -- Reset transistor,

23 Td -- Read-out transistor,

24 TH -- Level selection transistor,

25 VLIN -- Perpendicular signal line,

26 HLIN -- Level signal line.

27

28 PRIOR ART

29

30 [Description of the Prior Art] Drawing 12 shows the equal circuit of the CMOS solid
31 state camera (magnification mold CMOS image sensors) of the conventional example 1
32 equipped with the readout circuitry which a pixel signal can read for every pixel.

33 [0003] In drawing 12 , the unit cell of 1 pixel (1 pixel) / 1 unit is arranged in the shape of
34 [which is two dimensions] a matrix, and is formed in the cel field (image pick-up field).

35 [0004] Each unit cell consists of four transistors Ta, Tb, Tc, and Td and one photodiode
36 PD.

37 [0005] Namely, the photodiode PD with which touch-down potential is given to an anode
38 side The read-out transistor Td by which the end side is connected to the cathode side of
39 Photodiode PD (shutter gate transistor), The magnification transistor Tb by which the
40 gate is connected to the other end side of the read-out transistor Td The reset transistor Tc
41 by which the end side is connected to the gate of the perpendicular selection transistor
42 (line selection transistor) Ta and the magnification transistor Tb where the end side is
43 connected to the end side of the magnification transistor Tb is provided.

44 [0006] And corresponding to each pixel line, the perpendicular selection [which was
45 connected common to the gate of each read-out transistor Td of the unit cell of the same
46 line] line 6 connected with the line 4 common to the gate of each perpendicular selection

1 transistor Ta of the unit cell of the same line and the reset line 7 connected common to
2 the gate of each reset transistor Tc of the unit cell of the same line are formed in said cel
3 field by reading.

4 [0007] Moreover, corresponding to each pixel train, the power-source line 9 connected
5 common to the other end [of each reset transistor Tc of the unit cell of the same train as
6 the perpendicular signal line VLIN connected common to the other end side of each
7 magnification transistor Tb of the unit cell of the same train] and other end side of each
8 perpendicular selection transistor Ta is formed in said cel field.

9 [0008] Furthermore, in the exterior by the side of the end of a cel field, two or more load
10 transistors TL connected, respectively between one one end each of said perpendicular
11 signal line VLIN and a touch-down node are arranged horizontally.

12 [0009] Moreover, in the exterior by the side of the other end of a cel field, two or more
13 noise canceller circuits which consisted of two transistors TSH and TCLP and two
14 capacitors Cc and Ct are arranged horizontally.

15 [0010] And two or more level selection transistors TH connected to each other end side
16 of said perpendicular signal line VLIN through each above-mentioned noise canceller
17 circuit are arranged horizontally.

18 [0011] The level signal line HLIN is connected to each other end of the above-mentioned
19 level selection transistor TH in common, and they are a level reset transistor (not shown)
20 and the output amplifying circuit AMP in this level signal line HLIN. It connects.

21 [0012] In addition, the transistor TSH for sample hold by which, as for said each noise
22 canceller circuit, the end side was connected to the other end side of the perpendicular
23 signal line VLIN Coupling-capacitor Cc by which the end side was connected to the other
24 end side of the transistor TSH for these sample hold, The capacitor Ct for charge storages
25 connected between touch-down nodes the other end side of this coupling-capacitor Cc, It
26 is constituted by the transistor TCLP for a potential clamp connected to the connection
27 node of said capacitors Cc and Ct, and the end side of said level selection transistor TH is
28 connected to the connection node of said capacitors Cc and Ct.

29 [0013] furthermore, in the exterior of a cel field Two or more perpendicular selection
30 lines 6 of a cel field The timing generating circuit 10 which generates various kinds of
31 timing signals for supplying the perpendicular shift register 2 for carrying out a selection
32 control in scan, and said level selection transistor TH to the level shift register 3 for
33 driving in scan, said noise canceller circuit, etc., The bias generating circuit 11 for
34 generating predetermined bias potential at the end of the transistor TCLP for the potential
35 clamp of said noise canceller circuit etc., Pulse selector 2a for carrying out the selection
36 control of the output pulse of the above-mentioned perpendicular shift register 2, and
37 driving the perpendicular selection line 6 of each line of a cel field in scan is arranged,
38 respectively.

39 [0014] Drawing 13 is the timing wave form chart showing an example of actuation of the
40 solid-state image sensors shown in drawing 12 .

41 [0015] Next, actuation of the solid-state image sensors of drawing 12 is explained,
42 referring to drawing 13 .

43 [0016] The signal charge which photo electric conversion of the incident light of each
44 photodiode PD was carried out, and it produced is accumulated into Photodiode PD.

45 [0017] In a horizontal blanking interval, in case the signal charge of Photodiode PD is
46 read from the unit cell for a certain party, in order to choose each perpendicular signal

1 line VLIN, the line selection transistor Ta for a party is first turned ON by turning ON the
2 signal (phiADRES pulse) of the perpendicular selection line 6 of the line for selection.
3 [0018] The source follower circuit which consists of a magnification transistor Tb to
4 which the power-source potential VDD (for example, 3.3V) is supplied through the line
5 selection transistor Ta, and a load transistor TL in the unit cell for said party by this is
6 operated.
7 [0019] Next, in the unit cell for said party, reference voltage is outputted to the
8 perpendicular signal line VLIN by turning ON the signal (phiRESET pulse) of the reset
9 line 7, and carrying out fixed period reset of the gate voltage of the magnification
10 transistor Tb at reference voltage.
11 [0020] However, as described above, dispersion exists in the gate potential of the reset
12 magnification transistor Tb, and dispersion appears also in the reset potential of the
13 perpendicular signal line VLIN by the side of the other end.
14 [0021] Then, in order to reset dispersion in the reset potential of each perpendicular
15 signal line VLIN The driving signal (phiSH pulse) of the transistor TSH for sample hold
16 in a noise canceller circuit is turned ON beforehand (for example, the aforementioned
17 phiADRES to ON and coincidence of a pulse). After reference voltage is outputted to
18 said perpendicular signal line VLIN, by making the driving signal (phiCLP pulse) of the
19 transistor TCLP for a potential clamp fixed time amount ON, reference voltage is set as
20 the connection node of the capacitors Cc and Ct of a noise canceller circuit.
21 [0022] Next, aforementioned phiRESET After turning off a pulse, by choosing the read
22 line 4 of a predetermined line and turning on the signal (phiREAD pulse), the read-out
23 transistor Td is turned ON and gate potential is changed by reading the stored charge of
24 Photodiode PD to the gate of the magnification transistor Tb. The magnification
25 transistor Tb outputs the voltage signal according to the variation of gate potential to the
26 corresponding perpendicular signal line VLIN and a noise canceller circuit.
27 [0023] Then, a level effective scan term period can also accumulate the signal component
28 (signal level from which the noise was removed) equivalent to the difference of the
29 reference voltage read as described above, and a signal level in the capacitor Ct for
30 charge storages by turning off phiSH pulse in a noise canceller circuit.
31 [0024] That is, the noise mixed in the preceding paragraph side from noise canceller
32 circuits, such as dispersion in the reset potential of each perpendicular signal line VLIN
33 resulting from a cel field, is removed.
34 [0025] And phiADRES By the perpendicular selection transistor's Ta being controlled by
35 the OFF state, and changing a unit cell into the condition of not choosing, a cel field and
36 each noise canceller circuit are electrically separated by turning OFF a pulse.
37 [0026] By making sequential ON the driving signal (phiH pulse) of the level selection
38 transistor TH at a next horizontal effective scan period, the level selection transistor TH
39 is turned on [sequential], the signal level of the connection node (signal preservation
40 node) of said capacitors Cc and Ct is read to the level signal line HLIN one by one, and it
41 is the output amplifying circuit AMP. It is amplified and outputs.
42 [0027] It sets in the above-mentioned actuation and is the electrical potential difference
43 VVLIN of the perpendicular signal line VLIN. Noise rejection actuation which becomes
44 the operating voltage Vm (about 1.5 V) of a source follower circuit and which was
45 described in addition above is performed for every read-out actuation for every horizontal
46 line at a horizontal blanking interval.

1 [0028] Drawing 14 is the timing wave form chart showing the timing generating circuit
 2 10 in drawing 13 , the perpendicular shift register 2, and the example of pulse selector 2a
 3 of operation.
 4 [0029] Here, the case where the solid state camera of drawing 12 is used by 1 field =1 /
 5 30Hz (image of 30 frames per second which make the 1 field one frame) system is
 6 shown.
 7 [0030] The timing generating circuit 10 operates external input pulse signal phiVR and
 8 phiHP orthopedically in a buffer circuit, and is pulse signal phiVRR of a field period.
 9 Pulse signal phiHPV of a level period It inputs into said perpendicular shift register 2.
 10 [0031] The perpendicular shift register 2 is pulse signal phiVRR. Pulse signal phiHPV
 11 after an input clears all register outputs at the period of "L" level and makes it "L" level A
 12 shift action is performed, and the output pulse signal ROi (i=--, n, n+1, --) is made into
 13 "H" level one by one, and is inputted into said pulse selector 2a.
 14 [0032] Pulse selector 2a activates the signal (phiADRES pulse) of the perpendicular
 15 selection line 6, the signal (phiRESET pulse) of the reset line 7, and the signal (phiREAD
 16 pulse) of the read line 4, as shown in drawing 13 to each line for selection, and it scans
 17 the line for selection.
 18 [0033] It is each output pulse signal ROi of the perpendicular shift register 2 for the solid
 19 state camera of drawing 12 to carry out the selection control of the specific line for
 20 selection, as described above. It outputs only once within 1 field period. That is, since
 21 Photodiode PD performs signal read-out in the 1 field only once, the electronic shutter
 22 actuation which controls light-receiving time amount equivalent is impossible by
 23 controlling the signal storage time of Photodiode PD.
 24 [0034] On the other hand, drawing 15 shows roughly the configuration of the CMOS
 25 solid state camera of the conventional example 2 in which electronic shutter actuation is
 26 possible.
 27 [0035] This solid state camera For example, the image pick-up field 14 where the pixel
 28 cel 13 constituted as shown in drawing 12 has been arranged two-dimensional in the
 29 shape of a matrix (photo-electric-conversion section), Two or more perpendicular signal
 30 lines VLIN formed in the direction of a pixel train of said image pick-up field 14 Two or
 31 more perpendicular selection lines 6 for read-out control for controlling to be formed in
 32 the pixel line writing direction of said image pick-up field 14, and to read the photo-
 33 electric-conversion signal of each pixel cel 13 to said two or more perpendicular signal
 34 lines VLIN per pixel line, The 1st perpendicular selection circuitry 2 for carrying out a
 35 selection control in scan to the timing of read-out of said two or more perpendicular
 36 selection lines 6 for read-out control (perpendicular shift register for read-out), The level
 37 selection transistor TH for choosing said perpendicular signal line VLIN, The level
 38 selection circuitry 3 for carrying out the selection control of said level selection transistor
 39 (level selection shift register), Output amplifying circuit AMP for outputting the signal
 40 read to the level signal line HLIN and said level signal line HLIN for reading the signal
 41 of said perpendicular signal line VLIN chosen with said level selection shift register 3 It
 42 provides.
 43 [0036] In addition, especially the point equipped with a load transistor as shown in
 44 drawing 12 , a noise canceller circuit, etc. around the image pick-up field 14 although not
 45 illustrated is the same as that of the CMOS solid state camera of an example 1.
 46 [0037] Furthermore, the vertical-drive circuit (not shown) which generates the driving

1 signal for driving alternatively said two or more perpendicular selection lines 6 for read-
2 out control based on the output of the 2nd perpendicular selection circuitry (perpendicular
3 shift register for electronic shutters) 15 for carrying out a selection control in scan and
4 said 1st perpendicular selection circuitry and the output of the 2nd perpendicular
5 selection circuitry to the timing of signal are recording of said two or more perpendicular
6 selection lines 6 for read-out control is provided.

7 [0038] That is, the perpendicular shift register 15 for electronic shutters is formed
8 independently [the perpendicular shift register 2 for read-out], and it is constituted so
9 that this perpendicular shift register 15 for electronic shutters as well as the perpendicular
10 shift register 2 for read-out may scan the line for selection to predetermined timing.

11 [0039] Thereby, the perpendicular shift register 2 for read-out and the perpendicular shift
12 register 15 for electronic shutters enable it to carry out the selection control of the
13 specific line for selection to 2 times of timing within 1 field period.

14 [0040] Therefore, when the perpendicular shift register 15 for electronic shutters carries
15 out the selection control of the line for selection and starts are recording of a pixel signal
16 before the twist from which the perpendicular shift register 2 for read-out carries out the
17 selection control of the line for selection, and reads a pixel signal to the perpendicular
18 signal line VLIN, the electronic shutter actuation which controls light-receiving time
19 amount equivalent is attained.

20 [0041] By the way, the CMOS solid state camera of drawing 15 which has one
21 perpendicular shift register 2 for read-out and one perpendicular shift register 15 for
22 electronic shutters which were described above For example, when making the good
23 transformation child shutter actuation to which light-receiving time amount is changed
24 equivalent by changing the signal storage time automatically according to the output level
25 of a photo sensor perform There is a problem of the difference of the signal storage time
26 arising to pixel spacing, or changing the load of two perpendicular shift registers 2 and 15
27 to it according to the merits and demerits of the signal storage time.

28 [0042] This problem is explained below.

29 [0043] Drawing 16 shows an example in case the line selection timing of two
30 perpendicular shift registers 2 and 15 in drawing 15 is immobilization.

31 [0044] As shown in drawing 16 , the timing to which the perpendicular shift register 15
32 for electronic shutters performs line selection ahead of the perpendicular shift register 2
33 for read-out is being fixed, that is, the two above-mentioned perpendicular shift registers
34 2 and 15 of the time difference which performs line selection are always fixed.

35 [0045] Thus, when the line selection timing of two perpendicular shift registers 2 and 15
36 is immobilization, the perpendicular shift register 2 for read-out and the perpendicular
37 shift register 15 for electronic shutters begin selection of return and the following frame
38 to the first rank again, after it begins selection of a certain frame and the shift action from
39 the first rank to a tail end (that is, the number of pixels of the perpendicular direction of a
40 solid state camera) finishes.

41 [0046] Therefore, the solid state camera of drawing 15 has the problem of the difference
42 of the signal storage time arising to pixel spacing, or changing the load of two
43 perpendicular shift registers 2 and 15 to it according to the merits and demerits of the
44 signal storage time, when making the good transformation child shutter actuation to
45 which light-receiving time amount is changed equivalent by changing the signal storage
46 time automatically according to the output level of a photo sensor perform.

1 [0047] Here, said problem is stated to a detail, referring to drawing 17 about the case
2 where the merits and demerits of the time amount in which the perpendicular shift
3 register 15 for electronic shutters changes the timing (timing of an electronic shutter)
4 which performs line selection ahead of the perpendicular shift register 2 for read-out, and
5 accumulates a pixel signal as concrete technique for changing the signal storage time are
6 changed.

7 [0048] In drawing 17, a read-out control pulse is a signal which makes the shift action of
8 the perpendicular shift register 2 for read-out start, and a good transformation child
9 shutter control pulse is a signal which makes the shift action of the perpendicular shift
10 register 15 for electronic shutters start.

11 [0049] (1) After starting the shift action of the perpendicular shift register 15 for
12 electronic shutters by the control pulse of the electronic shutter generated to the timing t1
13 in drawing 17 on the occasion of selection of the 1st frame, before the shift action to a tail
14 end finishes (before choosing all pixel lines), in order to choose the 2nd frame to the
15 timing t3 in drawing 17, suppose that the electronic shutter pulse occurred. In this case,
16 the perpendicular shift register 15 for electronic shutters is reset to the above-mentioned
17 timing t3, and starts a shift action (line selection) from the first rank again.

18 [0050] Thereby, in case [at which it generated to the timing t2 in drawing 17] it reads,
19 and the shift action of the perpendicular shift register 2 for read-out begins by the control
20 pulse and said 1st frame is read, the difference of the signal storage time arises in the
21 pixel line by which selection assignment was not carried out with the pixel line by which
22 selection assignment was carried out with the perpendicular shift register 15 for
23 electronic shutters which the shift action started to said timing t1.

24 [0051] Thus, if the difference of the signal storage time arises, when a read-out output
25 level is changed depending on the location of a pixel line and displays the output signal
26 of a solid state camera on the screen of an image display device, it will become the cause
27 which image noises, such as a lateral stripe, generate.

28 [0052] (2) in the timing t4 in drawing 17, the shift action began to the selection line and
29 said timing t2 of the perpendicular shift register 15 for electronic shutters which the shift
30 action started to said timing t3 -- reading -- business -- since a total of two pixel lines of
31 the selection line of the perpendicular shift register 2 are chosen, these two pixel lines
32 serve as a load of two perpendicular shift registers 2 and 15.

33 [0053] on the other hand, in the timing t6 in drawing 17, the selection line by the
34 perpendicular shift register 15 for electronic shutters which the shift action started to said
35 timing t3 did not already exist, but the shift action started it to the timing t5 in drawing 17
36 -- reading -- business -- since one pixel line is chosen with the perpendicular shift register
37 2, this one pixel line serves as a load of two perpendicular shift registers 2 and 15.

38 [0054] Thus, if the load of two perpendicular shift registers 2 and 15 is changed
39 depending on electronic shutter timing, the voltage variation of power-source Rhine of a
40 solid state camera is imitated, and it comes, and when the output signal of a solid state
41 camera is displayed on the screen of an image display device, a lateral stripe will be
42 generated, and it will become the cause which worsens image quality notably.

43 [0055] In addition, the problem of the difference of the signal storage time arising to
44 pixel spacing, or changing the load of two perpendicular shift registers 2 and 15 to it
45 according to the merits and demerits of the signal storage time which was described

- 1 above is produced not only the solid state camera of a CMOS mold but when making the
- 2 solid state camera of a CCD mold perform good transformation child shutter actuation.

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ABSTRACT:

PROBLEM TO BE SOLVED: To provide a solid-state image pickup device capable of preventing the fluctuation of the loads of a vertical shift register for read and the vertical shift register for an electronic shutter in the case of performing an electronic shutter operation and preventing the generation of image noise such as horizontal stripes on the display screen of output signals.

SOLUTION: This device is provided with an image pickup area where a unit cell provided with a photodiode PD to be a pixel is two-dimensionally arranged, plural read lines 4 for driving the read transistor Td of each pixel row, plural vertical selection lines 6 for driving the vertical selection transistor Ta of each of the pixel rows, a vertical driving circuit 24 for selectively driving the plural read lines 4 and selectively driving the plural vertical selection lines 6, plural vertical signal lines VLIN for outputting signals from each unit cell of the successively driven pixel rows and row selection circuits 2, 21 and 22 for controlling the vertical driving circuit so as to successively drive the read transistor Td of each pixel two times at a desired signal storage timing and a signal read timing and to drive the vertical selection transistor Ta of the pixel row at the signal read timing.

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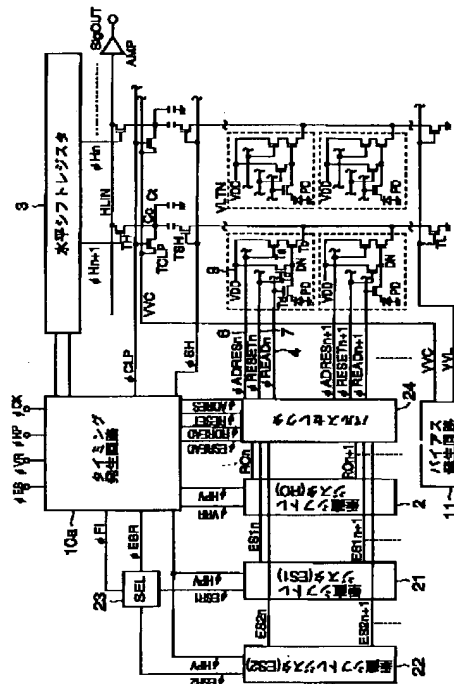
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(54) 【発明の名称】 固体撮像装置

(57) 【要約】

【課題】固体撮像装置の変可(連続)電子シャッタ動作を実現する。

【解決手段】画素となるフォトダイオードPDを有する単位セルが二次元的に配置された撮像領域と、各画素行の読み出しトランジスタTdを駆動するための複数本の読取り線4と、各画素行の垂直選択トランジスタTaを駆動するための複数本の垂直選択線6と、複数本の読取り線を選択的に駆動し、複数本の垂直選択線を選択的に駆動する垂直駆動回路24と、順次駆動された画素行の各单位セルから信号が出力する複数の垂直信号線VLINと、各画素行の読み出しトランジスタを所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に2回駆動させ、信号読み出しタイミングで画素行の垂直選択トランジスタを駆動させるように垂直駆動回路を制御する行選択回路2,21,22を具備する。



【特許請求の範囲】

【請求項1】 画素に対する入射光を光電変換して電荷を蓄積する光電変換手段、蓄積した電荷を検出部に読み出す読み出し手段、読み出された電荷を増幅する増幅手段、前記検出部の電荷をリセットするためのリセット手段および前記増幅手段から信号を出力させる垂直選択手段を有する単位セルが半導体基板上に二次元的に配置されてなり、複数の信号読み出し用の画素行および少なくとも2つのダミー画素行を有する撮像領域と、

前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各読み出し手段を駆動するための読み出し駆動信号を伝送するための複数の読取り線と、

前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各垂直選択手段を駆動するための行選択駆動信号を伝送するための複数の垂直選択線と、

前記複数の読取り線に読み出し駆動信号を選択的に供給して前記読み出し手段を駆動するとともに、前記複数の垂直選択線に行選択駆動信号を選択的に供給して前記垂直選択手段を駆動するための垂直駆動手段と、

前記撮像領域における各画素行の読み出し手段を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に2回駆動させるように前記垂直駆動手段を制御する行選択手段と、

前記撮像領域における各画素列に対応して設けられ、前記垂直駆動手段により順次駆動された画素行の各单位セルからそれぞれ出力される信号を垂直方向に伝送するための複数の垂直信号線とを具備し、

前記行選択手段は、

前記垂直駆動手段により前記複数の信号読み出し用の画素行の単位セルからの信号読み出しを制御した後、前記2つのダミー画素行のうちの第1のダミー画素行を駆動させるように選択制御し、前記垂直駆動手段により前記複数の信号読み出し用の画素行の単位セルにおける信号蓄積を制御した後、前記前記2つのダミー画素行のうちの第2のダミー画素行を駆動させるように選択制御することを特徴とする固体撮像装置。

【請求項2】 請求項1記載の固体撮像装置において、前記行選択手段は、

前記単位セルにおける信号蓄積の開始期間を制御するための電子シャッタ用のシフトレジスタと、

前記単位セルからの信号読み出しの開始期間を制御するための読み出し用のシフトレジスタを有し、

前記第1のダミー画素行は、前記読み出し用のシフトレジスタにより選択制御され、前記第2のダミー画素行は、前記電子シャッタ用のシフトレジスタにより選択制御されることを特徴とする固体撮像装置。

【請求項3】 画素に対する入射光を光電変換して電荷を蓄積する光電変換手段、蓄積した電荷を検出部に読み

出す読み出し手段、読み出された電荷を増幅する増幅手段、前記検出部の電荷をリセットするためのリセット手段および前記増幅手段から信号を出力させる垂直選択手段を有する単位セルが半導体基板上に二次元的に配置されてなり、複数の画素行を有する撮像領域と、

前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各読み出し手段を駆動するための読み出し駆動信号を伝送するための複数の読取り線と、

10 前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各垂直選択手段を駆動するための行選択駆動信号を伝送するための複数の垂直選択線と、

前記複数の読取り線に読み出し駆動信号を選択的に供給して前記読み出し手段を駆動するとともに、前記複数の垂直選択線に行選択駆動信号を選択的に供給して前記垂直選択手段を駆動するための垂直駆動手段と、

前記撮像領域における各画素行の読み出し手段を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に2回駆動させるように前記垂直駆動手段を制御する行選択手段と、

前記撮像領域における各画素列に対応して設けられ、前記垂直駆動手段により順次駆動された画素行の各单位セルからそれぞれ出力される信号を垂直方向に伝送するための複数の垂直信号線とを具備し、

前記行選択手段は、

前記垂直駆動手段により前記信号読み出しタイミングで前記各画素行の読み出し手段を駆動させる第1の手段と、

30 前記各画素行の読み出し手段を駆動させる少なくとも2個の第2の手段とを具備することを特徴とする固体撮像装置。

【請求項4】 請求項3記載の固体撮像装置において、前記撮像領域は、信号読み出し用の前記複数の画素行のほかに少なくとも3本のダミー画素行をさらに具備し、前記行選択手段は、前記第1の手段により前記ダミー画素行のうちの1つのダミー画素行を駆動させ、前記2個の第2の手段により前記ダミー画素行のうちの他の2つのダミー画素行を駆動させることを特徴とする固体撮像装置。

【請求項5】 請求項3または4記載の固体撮像装置において、

前記行選択手段は、各画素行の信号読み出しタイミングの周期に対応する1フィールド単位で1フィールド周期の期間内における信号蓄積タイミングを変化させることを特徴とする固体撮像装置。

【請求項6】 請求項5記載の固体撮像装置において、前記少なくとも2個の第2の手段は、互いに前記信号読み出しタイミングに対する信号蓄積タイミングを相対的に異ならせて前記読み出し手段を駆動させるものであ

り、前記第2の手段による前記垂直駆動手段の制御動作が1フィールド毎に交互に切換えられることを特徴とする固体撮像装置。

【請求項7】 請求項5記載の固体撮像装置において、前記行選択手段の第1の手段は、前記単位セルからの信号読み出しの開始期間を制御するための読み出し用のシフトレジスタを具備し、

前記行選択手段の第2の手段は、第1のフィールド期間での前記単位セルにおける信号蓄積の開始期間を制御するための第1の電子シャッタ用のシフトレジスタおよび前記第1のフィールド期間と交互に繰り返される第2のフィールド期間での前記単位セルにおける信号蓄積の開始期間を制御するための第2の電子シャッタ用のシフトレジスタを具備することを特徴とする固体撮像装置。

【請求項8】 請求項1乃至7のいずれか1つに記載の固体撮像装置において、

前記行選択手段は、前記撮像領域における各画素行の読み出し手段を2回駆動させる際、前記光電変換手段の周辺で前記読取り線に隣接する他の配線の電圧を前記2回の駆動時とも実質的に同一にするように前記垂直駆動手段を制御することを特徴とする固体撮像装置。

【請求項9】 請求項8記載の固体撮像装置において、前記読取り線に隣接する他の配線は、前記垂直選択線であることを特徴とする固体撮像装置。

【請求項10】 半導体基板上の撮像領域に二次元的に配置された単位セルの光電変換素子から蓄積電荷を読み出す際、この読み出しを制御する配線を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に2回駆動させ、前記信号読み出しタイミングで読み出された信号を出力させる電子シャッタ動作を行う固体撮像装置において、

前記読み出しを制御する配線に隣接し、前記光電変換素子の周辺に存在する他の配線の電圧を前記信号蓄積タイミングと信号読み出しタイミングとで実質的に同一にすることを特徴とする固体撮像装置。

【請求項11】 請求項1乃至10のいずれか1つに記載の固体撮像装置において、

前記単位セルは、

アノード側に接地電位が与えられる1個のフォトダイオードと、

前記1個のフォトダイオードのカソード側に一端側が接続され、ゲートに読取り線が接続された1個の読み出しトランジスタと、

前記読み出しトランジスタの他端側にゲートが接続され、一端側に垂直信号線が接続された1個の増幅トランジスタと、

前記増幅トランジスタの他端側に一端側が接続され、ゲートには垂直選択線が接続された1個の垂直選択トランジスタと、

前記垂直選択トランジスタの他端側に接続された1本の

電源線と、

前記増幅トランジスタのゲートと前記電源線との間に接続され、ゲートにはリセット線が接続された1個のリセットトランジスタとを具備し、前記1個のフォトダイオードが1つの画素に対応することを特徴とする固体撮像装置。

【請求項12】 2画素/1ユニットの単位セルが半導体基板上に二次元的に配置されてなる撮像領域を有する固体撮像装置において、

10 前記撮像領域の単位セルにおける2画素の光電変換素子からそれぞれ蓄積電荷を読み出す際、この読み出しを制御する配線に隣接し、前記光電変換素子の周辺に存在する他の配線の電圧を各画素の読み出し時で実質的に同一にすることを特徴とする固体撮像装置。

【請求項13】 請求項1乃至12のいずれか1つに記載の固体撮像装置において、

前記単位セルは、

各アノード側に接地電位が与えられる2個のフォトダイオードと、

20 前記2個のフォトダイオードの各カソード側にそれぞれ対応して各一端側が接続され、各ゲートに2本の読取り線がそれぞれ対応して接続された2個の読み出しトランジスタと、

前記2個の読み出しトランジスタの各他端側に共通にゲートが接続され、一端側に垂直信号線が接続された1個の増幅トランジスタと、

前記増幅トランジスタの他端側に一端側が接続され、ゲートには前記垂直選択線が接続された1個の垂直選択トランジスタと、

30 前記垂直選択トランジスタの他端側に接続された1本の電源線と、

前記増幅トランジスタのゲートと前記電源線との間に接続され、ゲートにはリセット線が接続された1個のリセットトランジスタを具備し、

前記2個のフォトダイオードが2つの画素に対応することを特徴とする固体撮像装置。

【発明の詳細な説明】

【0001】

40 【発明の属する技術分野】本発明は、固体撮像装置に係り、特に固体撮像装置の可変電子シャッタ制御回路および画素信号読み出し制御回路に関するもので、例えばビデオカメラ、電子スチールカメラなどに使用される。

【0002】

【従来の技術】図12は、1画素毎に画素信号の読み出しが可能な読み出し回路を備えた従来例1のCMOS固体撮像装置（増幅型CMOSイメージセンサ）の等価回路を示している。

50 【0003】図12において、セル領域（撮像領域）には1ピクセル（1画素）/1ユニットの単位セルが二次元の行列状に配置されて形成されている。

【0004】各单位セルは、例えば4個のトランジスタTa、Tb、Tc、Tdと、1個のフォトダイオードPDから構成される。

【0005】即ち、アノード側に接地電位が与えられるフォトダイオードPDと、フォトダイオードPDのカソード側に一端側が接続されている読み出しトランジスタ（シャッタゲートトランジスタ）Tdと、読み出しトランジスタTdの他端側にゲートが接続されている増幅トランジスタTbと、増幅トランジスタTbの一端側に一端側が接続されている垂直選択トランジスタ（行選択トランジスタ）Taと、増幅トランジスタTbのゲートに一端側が接続されているリセットトランジスタTcとを具備する。

【0006】そして、前記セル領域には、各画素行に対応して、同一行の単位セルの各読み出しトランジスタTdのゲートに共通に接続された読取り線4と、同一行の単位セルの各垂直選択トランジスタTaのゲートに共通に接続された垂直選択線6と、同一行の単位セルの各リセットトランジスタTcのゲートに共通に接続されたリセット線7が形成されている。

【0007】また、前記セル領域には、各画素列に対応して、同一列の単位セルの各増幅トランジスタTbの他端側に共通に接続された垂直信号線VLINと、同一列の単位セルの各リセットトランジスタTcの他端側および各垂直選択トランジスタTaの他端側に共通に接続された電源線9が形成されている。

【0008】さらに、セル領域の一端側の外部には、前記垂直信号線VLINの各一端側と接地ノードとの間にそれぞれ接続された複数の負荷トランジスタTLが水平方向に配置されている。

【0009】また、セル領域の他端側の外部には、例えば2個のトランジスタTSH、TCLPと2個のコンデンサCc、Ctから構成された複数のノイズキャンセラ回路が水平方向に配置されている。

【0010】そして、上記各ノイズキャンセラ回路を介して前記垂直信号線VLINの各他端側に接続された複数の水平選択トランジスタTHが水平方向に配置されている。

【0011】上記水平選択トランジスタTHの各他端に共通に水平信号線HLINが接続されており、この水平信号線HLINには水平リセットトランジスタ（図示せず）および出力増幅回路AMPが接続されている。

【0012】なお、前記各ノイズキャンセラ回路は、垂直信号線VLINの他端側に一端側が接続されたサンプルホールド用のトランジスタTSHと、このサンプルホールド用のトランジスタTSHの他端側に一端側が接続された結合コンデンサCcと、この結合コンデンサCcの他端側と接地ノードとの間に接続された電荷蓄積用のコンデンサCtと、前記コンデンサCc、Ctの接続ノードに接続された電位クランプ用のトランジスタTCLPとにより構

成されており、前記コンデンサCc、Ctの接続ノードに前記水平選択トランジスタTHの一端側が接続されている。

【0013】さらに、セル領域の外部には、セル領域の複数の垂直選択線6を走査的に選択制御するための垂直シフトレジスタ2、前記水平選択トランジスタTHを走査的に駆動するための水平シフトレジスタ3、前記ノイズキャンセラ回路などに供給するための各種のタイミング信号を発生するタイミング発生回路10と、前記ノイズキャンセラ回路の電位クランプ用のトランジスタTCLPの一端などに所定のバイアス電位を発生するためのバイアス発生回路11と、上記垂直シフトレジスタ2の出力パルスを選択制御してセル領域の各行の垂直選択線6を走査的に駆動するためのパルスセクタ2aとがそれぞれ配置されている。

【0014】図13は、図12に示した固体イメージセンサの動作の一例を示すタイミング波形図である。

【0015】次に、図13を参照しながら、図12の固体イメージセンサの動作を説明する。

20 【0016】各フォトダイオードPDの入射光が光電変換されて生じた信号電荷はフォトダイオードPD内に蓄積される。

【0017】水平帰線期間において、ある一行分の単位セルからフォトダイオードPDの信号電荷を読み出す際、まず、各垂直信号線VLINを選択するために、選択対象行の垂直選択線6の信号（φADRES パルス）をオンにすることにより一行分の行選択トランジスタTaをオンにする。

30 【0018】これにより、前記一行分の単位セルにおいて、行選択トランジスタTaを介して電源電位VDD（例えば3.3V）が供給される増幅トランジスタTbと負荷トランジスタTLからなるソースフォロフ回路を動作させる。

【0019】次に、前記一行分の単位セルにおいて、リセット線7の信号（φRESET パルス）をオンにし、増幅トランジスタTbのゲート電圧を基準電圧に一定期間リセットすることにより、垂直信号線VLINに基準電圧を出力する。

40 【0020】しかし、前記したようにリセットされた増幅トランジスタTbのゲート電位にはばらつきが存在し、その他端側の垂直信号線VLINのリセット電位にもばらつきが現われる。

【0021】そこで、各垂直信号線VLINのリセット電位のばらつきをリセットするために、予め（例えば前記φADRES パルスのオンと同時に）ノイズキャンセラ回路におけるサンプルホールド用トランジスタTSHの駆動信号（φSHパルス）をオンにしておき、前記垂直信号線VLINに基準電圧が出力された後に電位クランプ用のトランジスタTCLPの駆動信号（φCLP パルス）を一定時間オンにすることにより、ノイズキャンセラ回路のコンデンサC

c、Ctの接続ノードに基準電圧を設定する。

【0022】次に、前記RESETパルスをオフした後、所定行の読取り線4を選択してその信号(ϕ READパルス)をオンすることにより、読み出しトランジスタTdをオンにし、フォトダイオードPDの蓄積電荷を増幅トランジスタTbのゲートに読み出すことによりゲート電位を変化させる。増幅トランジスタTbは、ゲート電位の変化量に応じた電圧信号を対応する垂直信号線VLINおよびノイズキャンセラ回路に出力する。

【0023】この後、ノイズキャンセラ回路における ϕ SHパルスをオフすることにより、前記したように読み出された基準電圧と信号電圧の差分に相当する信号成分(ノイズが除去された信号電圧)を電荷蓄積用のコンデンサCcに水平有効走査期間中も蓄積することができる。

【0024】つまり、セル領域に起因する各垂直信号線VLINのリセット電位のばらつきなどのノイズキャンセラ回路より前段側に混入したノイズは除去される。

【0025】そして、 ϕ ADRESパルスをオフにすることにより垂直選択トランジスタTaがオフ状態に制御されて単位セルが非選択状態にされることにより、セル領域と各ノイズキャンセラ回路とが電氣的に分離される。

【0026】この後の水平有効走査期間に水平選択トランジスタTHの駆動信号(ϕ Hパルス)を順次オンにすることにより、水平選択トランジスタTHが順次オンになり、前記コンデンサCc、Ctの接続ノード(信号保存ノード)の信号電圧が水平信号線HLINに順次読み出され、出力増幅回路AMPにより増幅されて出力する。

【0027】上記動作において、垂直信号線VLINの電圧VVLINは、水平帰線期間にはソースホロワ回路の動作電圧Vm(約1.5V)になる。なお、前記したノイズ除去動作は1水平線毎の読み出し動作毎に行われる。

【0028】図14は、図13中のタイミング発生回路10、垂直シフトレジスタ2およびパルスセクタ2aの動作例を示すタイミング波形図である。

【0029】ここでは、図12の固体撮像装置が1フィールド=1/30Hz(1フィールドを1フレームとする30フレーム/秒の画像)のシステムで使用される場合を示している。

【0030】タイミング発生回路10は、外部入力パルス信号 ϕ VRと ϕ HPをバッファ回路で整形し、フィールド周期のパルス信号 ϕ VRRと水平周期のパルス信号 ϕ HPVを前記垂直シフトレジスタ2へ入力する。

【0031】垂直シフトレジスタ2は、パルス信号 ϕ VR入力が“L”レベルの期間にレジスタ出力を全てクリアして“L”レベルにした後、パルス信号 ϕ HPVによりシフト動作を行って出力パルス信号R0i(i=...,n,n+1,...)を順次“H”レベルにし、前記パルスセクタ2aに入力する。

【0032】パルスセクタ2aは、各選択対象行に対して垂直選択線6の信号(ϕ ADRESパルス)、リセット線7の信号(ϕ RESETパルス)、読取り線4の信号(ϕ READパルス)を図13に示したように活性化し、選択対象行を走査する。

【0033】上記したように、図12の固体撮像装置は、特定の選択対象行を選択制御するための垂直シフトレジスタ2の各出力パルス信号R0iを、1フィールド期間内に1回しか出力しない。即ち、フォトダイオードPDは、1フィールドに1回しか信号読み出しを行わないので、フォトダイオードPDの信号蓄積時間を制御することによって等価的に受光時間を制御する電子シャッタ動作は不可能である。

【0034】一方、図15は、電子シャッタ動作が可能な従来例2のCMOS固体撮像装置の構成を概略的に示している。

【0035】この固体撮像装置は、例えば図12に示したように構成される画素セル13が行列状に二次元的に配置された撮像領域(光電変換部)14と、前記撮像領域14の画素列方向に形成された複数の垂直信号線VLINと、前記撮像領域14の画素行方向に形成され、画素行単位で各画素セル13の光電変換信号を前記複数の垂直信号線VLINに読み出すように制御するための複数の読み出し制御用垂直選択線6と、前記複数の読み出し制御用垂直選択線6を読み出しのタイミングで走査的に選択制御するための第1の垂直選択回路(読み出し用垂直シフトレジスタ)2と、前記垂直信号線VLINを選択するための水平選択トランジスタTHと、前記水平選択トランジスタを選択制御するための水平選択回路(水平選択シフトレジスタ)3と、前記水平選択シフトレジスタ3により選択された前記垂直信号線VLINの信号を読み出すための水平信号線HLINと、前記水平信号線HLINに読み出された信号を出力するための出力増幅回路AMPとを具備している。

【0036】なお、特に図示していないが、図12に示されるような負荷トランジスタやノイズキャンセラ回路などを撮像領域14の周辺に備える点は、実施例1のCMOS固体撮像装置と同様である。

【0037】さらに、前記複数の読み出し制御用垂直選択線6を信号蓄積のタイミングで走査的に選択制御するための第2の垂直選択回路(電子シャッタ用垂直シフトレジスタ)15と、前記第1の垂直選択回路の出力および第2の垂直選択回路の出力に基づいて前記複数の読み出し制御用垂直選択線6を選択的に駆動するための駆動信号を生成する垂直駆動回路(図示せず)とを具備する。

【0038】即ち、読み出し用の垂直シフトレジスタ2とは別に電子シャッタ用の垂直シフトレジスタ15が設けられており、この電子シャッタ用垂直シフトレジスタ15も所定のタイミングで読み出し用垂直シフトレジ

タ2と同様に選択対象行を走査するように構成されている。

【0039】これにより、読み出し用の垂直シフトレジスタ2および電子シャッタ用垂直シフトレジスタ15により、1フィールド期間内に2回のタイミングで特定の選択対象行を選択制御することが可能になる。

【0040】したがって、読み出し用垂直シフトレジスタ2が選択対象行を選択制御して画素信号を垂直信号線VLINに読み出すより前に、電子シャッタ用垂直シフトレジスタ15が選択対象行を選択制御して画素信号の蓄積を開始することにより、等価的に受光時間を制御する電子シャッタ動作が可能になる。

【0041】ところで、上記したような1個の読み出し用垂直シフトレジスタ2および1個の電子シャッタ用垂直シフトレジスタ15を有する図15のCMOS固体撮像装置は、例えば受光センサの出力レベルに応じて自動的に信号蓄積時間を変化させることによって等価的に受光時間を変化させる可変電子シャッタ動作を行わせる場合に、信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じたり、2つの垂直シフトレジスタ2、15の負荷が変動するという問題がある。

【0042】この問題について、以下に説明する。

【0043】図16は、図15中の2つの垂直シフトレジスタ2、15の行選択タイミングが固定である場合の一例を示す。

【0044】図16に示すように、電子シャッタ用垂直シフトレジスタ15が読み出し用垂直シフトレジスタ2よりも先に行選択を行うタイミングが固定されている、つまり、上記2つの垂直シフトレジスタ2、15が行選択を行う時間差は常に一定である。

【0045】このように2つの垂直シフトレジスタ2、15の行選択タイミングが固定であった場合には、読み出し用垂直シフトレジスタ2および電子シャッタ用垂直シフトレジスタ15は、あるフレームの選択を始めて初段から終段まで（つまり、固体撮像装置の垂直方向の画素数）のシフト動作が終わると再び初段に戻り、次のフレームの選択を始める。

【0046】したがって、図15の固体撮像装置は、例えば受光センサの出力レベルに応じて自動的に信号蓄積時間を変化させることによって等価的に受光時間を変化させる可変電子シャッタ動作を行わせる場合に、信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じたり、2つの垂直シフトレジスタ2、15の負荷が変動するという問題がある。

【0047】ここで、信号蓄積時間を変化させるための具体的な手法として、電子シャッタ用垂直シフトレジスタ15が読み出し用垂直シフトレジスタ2よりも先に行選択を行うタイミング（電子シャッタのタイミング）を変化させて画素信号の蓄積を行う時間の長短を変化させる場合について、図17を参照しながら前記問題につい

て詳細に述べる。

【0048】図17において、読み出し制御パルスは読み出し用垂直シフトレジスタ2のシフト動作を開始させる信号であり、可変電子シャッタ制御パルスは電子シャッタ用垂直シフトレジスタ15のシフト動作を開始させる信号である。

【0049】（1）第1のフレームの選択に際して図17中のタイミングt1で発生した電子シャッタの制御パルスにより電子シャッタ用垂直シフトレジスタ15のシフト動作を開始した後、終段までのシフト動作が終わる前（全ての画素行を選択する前）に、図17中のタイミングt3で第2のフレームを選択するために電子シャッタパルスが発生したとする。この場合、電子シャッタ用垂直シフトレジスタ15は上記タイミングt3でリセットされ、再び初段からシフト動作（行選択）を開始する。

【0050】これにより、図17中のタイミングt2で発生した読み出し制御パルスにより読み出し用垂直シフトレジスタ2のシフト動作が開始して前記第1のフレームの読み出しを行う際、前記タイミングt1でシフト動作が開始した電子シャッタ用垂直シフトレジスタ15によって選択指定された画素行と選択指定されなかった画素行とでは信号蓄積時間の差が生じる。

【0051】このように信号蓄積時間の差が生じると、読み出し出力レベルが画素行の位置に依存して変動し、固体撮像装置の出力信号を画像表示装置の画面に表示した場合に横筋などの画像ノイズが発生する原因となる。

【0052】（2）図17中のタイミングt4では、前記タイミングt3でシフト動作が開始した電子シャッタ用垂直シフトレジスタ15の選択行と前記タイミングt2でシフト動作が開始した読み出し用垂直シフトレジスタ2の選択行の計2本の画素行が選択されるので、この2本の画素行が2つの垂直シフトレジスタ2、15の負荷となる。

【0053】これに対して、図17中のタイミングt6では、前記タイミングt3でシフト動作が開始した電子シャッタ用垂直シフトレジスタ15による選択行は既に存在せず、図17中のタイミングt5でシフト動作が開始した読み出し用垂直シフトレジスタ2により1本の画素行が選択されるので、この1本の画素行が2つの垂直シフトレジスタ2、15の負荷となる。

【0054】このように2つの垂直シフトレジスタ2、15の負荷が電子シャッタタイミングに依存して変動すると、固体撮像装置の電源ラインの電圧変動をまねき、固体撮像装置の出力信号を画像表示装置の画面に表示した場合に横筋が発生し、顕著に画質を悪くする原因となる。

【0055】なお、上記したような信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じたり、2つの垂直シフトレジスタ2、15の負荷が変動するという問題は、CMOS型の固体撮像装置に限らず、CCD型

の固体撮像装置で可変電子シャッタ動作を行わせる場合にも生じる。

【0056】

【発明が解決しようとする課題】上記したように従来の固体撮像装置は、信号蓄積時間を変化させて可変電子シャッタ動作を行わせる場合に信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じたり、読み出し用垂直シフトレジスタと電子シャッタ用垂直シフトレジスタの負荷が変動し、出力信号の表示画面に横筋などの画像ノイズが発生する原因となるという問題があった。

【0057】本発明は上記の問題点を解決すべくなされたもので、電子シャッタ動作を行わせる場合に読み出し用垂直シフトレジスタと電子シャッタ用垂直シフトレジスタの負荷の変動を防止でき、出力信号の表示画面における横筋などの画像ノイズの発生を防止し得る固体撮像装置を提供することを目的とする。

【0058】また、本発明は、フィールド単位で画素の信号蓄積時間を変化させる可変電子シャッタ動作（連続電子シャッタ動作）を行わせる場合に読み出し用垂直シフトレジスタと電子シャッタ用垂直シフトレジスタの負荷の変動を防止でき、出力信号の表示画面における横筋などの画像ノイズの発生を防止し得る固体撮像装置を提供することを目的とする。

【0059】また、本発明は、連続電子シャッタ動作を行わせる場合に信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じることを防止し得る固体撮像装置を提供することを目的とする。

【0060】また、本発明は、連続電子シャッタ動作を行わせる場合に、出力信号の表示画面における横筋などの画像ノイズの発生を防止し得る固体撮像装置を提供することを目的とする。

【0061】また、本発明は、画素で光電変換・蓄積された信号を読み出す際に、画素周辺の配線から容量結合によりノイズが飛び込むことを防止し得る固体撮像装置を提供することを目的とする。

【0062】

【課題を解決するための手段】本発明の第1の固体撮像装置は、画素に対する入射光を光電変換して電荷を蓄積する光電変換手段、蓄積した電荷を検出部に読み出す読み出し手段、読み出された電荷を増幅する増幅手段、前記検出部の電荷をリセットするためのリセット手段および前記増幅手段から信号を出力させる垂直選択手段を有する単位セルが半導体基板上に二次元的に配置されてなり、複数の信号読み出し用の画素行および少なくとも2つのダミー画素行を有する撮像領域と、前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各読み出し手段を駆動するための読み出し駆動信号を伝送するための複数の読取り線と、前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セル

の各垂直選択手段を駆動するための行選択駆動信号を伝送するための複数の垂直選択線と、前記複数の読取り線に読み出し駆動信号を選択的に供給して前記読み出し手段を駆動するとともに、前記複数の垂直選択線に行選択駆動信号を選択的に供給して前記垂直選択手段を駆動するための垂直駆動手段と、前記撮像領域における各画素行の読み出し手段を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に2回駆動させるように前記垂直駆動手段を制御する行選択手段と、前記撮像領域における各画素列に対応して設けられ、前記垂直駆動手段により順次駆動された画素行の各単位セルからそれぞれ出力される信号を垂直方向に伝送するための複数の垂直信号線とを具備し、前記行選択手段は、前記垂直駆動手段により前記複数の信号読み出し用の画素行の単位セルからの信号読み出しを制御した後、前記2つのダミー画素行のうちの第1のダミー画素行を駆動させるように選択制御し、前記垂直駆動手段により前記複数の信号読み出し用の画素行の単位セルにおける信号蓄積を制御した後、前記前記2つのダミー画素行のうちの第2のダミー画素行を駆動させるように選択制御することを特徴とする。

【0063】本発明の第2の固体撮像装置は、画素に対する入射光を光電変換して電荷を蓄積する光電変換手段、蓄積した電荷を検出部に読み出す読み出し手段、読み出された電荷を増幅する増幅手段、前記検出部の電荷をリセットするためのリセット手段および前記増幅手段から信号を出力させる垂直選択手段を有する単位セルが半導体基板上に二次元的に配置されてなり、複数の画素行を有する撮像領域と、前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各読み出し手段を駆動するための読み出し駆動信号を伝送するための複数の読取り線と、前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各垂直選択手段を駆動するための行選択駆動信号を伝送するための複数の垂直選択線と、前記複数の読取り線に読み出し駆動信号を選択的に供給して前記読み出し手段を駆動するとともに、前記複数の垂直選択線に行選択駆動信号を選択的に供給して前記垂直選択手段を駆動するための垂直駆動手段と、前記撮像領域における各画素行の読み出し手段を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に2回駆動させるように前記垂直駆動手段を制御する行選択手段と、前記撮像領域における各画素列に対応して設けられ、前記垂直駆動手段により順次駆動された画素行の各単位セルからそれぞれ出力される信号を垂直方向に伝送するための複数の垂直信号線とを具備し、前記行選択手段は、前記垂直駆動手段により前記信号読み出しタイミングで前記各画素行の読み出し手段を駆動させる第1の手段と、前記垂直駆動手段により前記信号蓄積タイミングで前記各画素行の読み出し手

段を駆動させる少なくとも2個の第2の手段とを具備することを特徴とする。

【0064】本発明の第3の固体撮像装置は、前記第2の固体撮像装置において、前記撮像領域は、信号読み出し用の前記複数の画素行のほかに少なくとも3本のダミー画素行をさらに具備し、前記行選択手段は、前記第1の手段により前記ダミー画素行のうちの1つのダミー画素行を駆動させ、前記2個の第2の手段により前記ダミー画素行のうちの他の2つのダミー画素行を駆動させることを特徴とする。

【0065】本発明の第4の固体撮像装置は、前記第2または第3の固体撮像装置において、前記行選択手段は、各画素行の信号読み出しタイミングの周期に対応する1フィールド単位で1フィールド周期の期間内における信号蓄積タイミングを変化させることを特徴とする。

【0066】本発明の第5の固体撮像装置は、前記第4の固体撮像装置において、前記少なくとも2個の第2の手段は、互いに前記信号読み出しタイミングに対する信号蓄積タイミングを相対的に異ならせて前記読み出し手段を駆動させるものであり、前記第2の手段による前記垂直駆動手段の制御動作が1フィールド毎に交互に切換えられることを特徴とする。

【0067】本発明の第6の固体撮像装置は、前記第1乃至第5のいずれか1つの固体撮像装置において、前記行選択手段は、前記撮像領域における各画素行の読み出し手段を2回駆動させる際、前記光電変換手段の周辺で前記読取り線に隣接する他の配線の電圧を前記2回の駆動時とも実質的に同一にするように前記垂直駆動手段を制御することを特徴とする。

【0068】本発明の第7の固体撮像装置は、半導体基板上の撮像領域に二次元的に配置された単位セルの光電変換素子から蓄積電荷を読み出す際、この読み出しを制御する配線を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に2回駆動させ、前記信号読み出しタイミングで読み出された信号を出力させる電子シャッタ動作を行う固体撮像装置において、前記読み出しを制御する配線に隣接し、前記光電変換素子の周辺に存在する他の配線の電圧を前記信号蓄積タイミングと信号読み出しタイミングとで実質的に同一にすることを特徴とする。

【0069】本発明の第8の固体撮像装置は、2画素/1ユニットの単位セルが半導体基板上に二次元的に配置されてなる撮像領域を有する固体撮像装置において、前記撮像領域の単位セルにおける2画素の光電変換素子からそれぞれ蓄積電荷を読み出す際、この読み出しを制御する配線に隣接し、前記光電変換素子の周辺に存在する他の配線の電圧を各画素の読み出し時に実質的に同一にすることを特徴とする。

【0070】

【発明の実施の形態】以下、図面を参照して本発明の実

施の形態を詳細に説明する。

【0071】＜第1の実施の形態＞図1は、第1の実施の形態の増幅型CMOS固体撮像装置の等価回路を示している。

【0072】図1のCMOS固体撮像装置は、図15を参照して前述した従来例2のCMOS固体撮像装置と比べて、大部分は同様であるが、読み出し用の垂直シフトレジスタ2aおよび電子シャッタ用の垂直シフトレジスタ15aなどが異なり、その他は同じであるので図15中と同一符号を付している。

【0073】即ち、図1のCMOS固体撮像装置は、例えば図12の従来例1で示したように構成される画素セル13が行列状に二次元的に配置された撮像領域（光電変換部）14と、前記撮像領域14の画素列方向に形成された複数の垂直信号線VLINと、前記撮像領域14の画素行方向に形成され、画素行単位で各画素セル13の光電変換信号を前記複数の垂直信号線VLINに読み出すように制御するための複数の読み出し制御用垂直選択線6と、前記複数の読み出し制御用垂直選択線6を読み出しのタイミングで走査的に選択制御するための第1の垂直選択回路（読み出し用垂直シフトレジスタ）2aと、前記複数の読み出し制御用垂直選択線6を信号蓄積のタイミングで走査的に選択制御するための第2の垂直選択回路（電子シャッタ用垂直シフトレジスタ）15aと、前記第1の垂直選択回路2aの出力および第2の垂直選択回路15aの出力に基づいて前記複数の読み出し制御用垂直選択線6を選択的に駆動するための駆動信号を生成する垂直駆動回路（パルスセレクト）16と、前記垂直信号線VLINを選択するための水平選択トランジスタTHと、前記水平選択トランジスタTHを選択制御するための水平選択回路（水平選択シフトレジスタ）3と、前記水平選択シフトレジスタ3により選択された前記垂直信号線VLINの信号を読み出すための水平信号線HLINと、前記水平信号線HLINに読み出された信号を出力するための出力増幅回路AMPとを具備している。

【0074】なお、図15の従来例2のCMOS固体撮像装置と同様に、ここでは特に図示されていないが、図12に示されるような負荷トランジスタやノイズキャンセラ回路などを撮像領域14の周辺に備えている。

【0075】そして、さらに、

(1) 前記撮像領域14に本来の画素行とは別に2本のダミー画素行（第1のダミー画素行141および第2のダミー画素行142）が付加されている。(2) 前記読み出し用の垂直シフトレジスタ（第1の垂直シフトレジスタ）2aは、撮像領域14の本来の画素行数+1のシフト段数を有し、前記電子シャッタ用の垂直シフトレジスタ（第2の垂直シフトレジスタ）15aも、撮像領域14の本来の画素行数+1のシフト段数を有する。

(3) 垂直駆動回路16は、読み出し用の垂直シフトレジスタ2aの最終段出力信号を選択して前記第1のダミ

一画素行141に供給し、電子シャッタ用の垂直シフトレジスタ15aの最終段出力信号を選択して前記第2のダミー画素行142に供給するように構成されている。

【0076】前記2本のダミー画素行141、142は、本来の画素行と同じ構成であるが、垂直駆動回路16により選択された時に負荷として作用するために付加されたものである。

【0077】図1の固体撮像装置においては、電子シャッタ用の垂直シフトレジスタ15aおよび読み出し用の垂直シフトレジスタ2aにより、同じ垂直選択線を1フ

ィールド期間内に2回選択制御することが可能であり、画素（フォトダイオード）の信号蓄積時間を制御するシャッタ動作を行うことができる。

【0078】この場合、電子シャッタ用の垂直シフトレジスタ15aは、信号蓄積の開始タイミングを制御するシフトクロック信号に基づいてシフト動作を行い、シャッタ動作期間には各対応する画素行を選択制御して画素の信号蓄積を行わせる（読み出しは行わない）ように制御し、シャッタ動作期間以外（画素行の選択終了後から次の選択開始までの期間）は第2のダミー画素行142を選択制御する。

【0079】また、読み出し用の垂直シフトレジスタ2aは、信号読み出しの開始タイミングを制御するシフトクロック信号に基づいてシフト動作を行い、垂直期間内の垂直有効走査期間における各水平期間には各対応する画素行を選択制御し、垂直帰線期間には第1のダミー画素行141を選択制御する。

【0080】即ち、上記第1の実施の形態の固体撮像装置によれば、垂直駆動回路16は、読み出し用の垂直シフトレジスタ2aおよび電子シャッタ用の垂直シフトレジスタ15aの各出力にそれぞれ対応して1本ずつ（合計2本）の画素行を常に選択駆動しており、常に選択負荷が等しいので、選択負荷の大小による読み出しレベルの変動に起因する表示画面上の横縞の発生を防ぐことができる。

【0081】＜第2の実施の形態＞図2は、第2の実施の形態の増幅型CMOS固体撮像装置の等価回路を示している。

【0082】図2のCMOS固体撮像装置は、図1を参照して前述した第1の実施の形態のCMOS固体撮像装置に対して、（1）前記撮像領域14にさらに1本のダミー画素行（第3のダミー画素行143）が追加されている点、（2）さらに、電子シャッタ用の垂直シフトレジスタ15aと同じシフト段数を有する1個の電子シャッタ用の垂直シフトレジスタ15bが追加され、その各段出力が前記電子シャッタ用の垂直シフトレジスタ15aの各段出力とフィールド単位で切り換え選択されて垂直駆動回路（パルスセクタ）16aで使用される点、（3）垂直駆動回路16aは、3個の垂直シフトレジスタ2a、15a、15bの出力に基づいて前記複数の読

み出し制御用垂直選択線6を選択的に駆動するための駆動信号を生成する点、（4）垂直駆動回路16aは、追加された電子シャッタ用の垂直シフトレジスタ15bの最終段出力信号を選択して前記第3のダミー画素行143に供給する点が若干異なり、その他は同じであるので図1中と同一符号を付している。

【0083】図3は、図2の固体撮像装置において2個の電子シャッタ用垂直シフトレジスタ15a、15bがフィールド単位で交互に電子シャッタ動作を制御する様子を示すタイミング図である。

【0084】図3に示すタイミング図から分かるように、図2の固体撮像装置においては、電子シャッタ専用の2個の垂直シフトレジスタ15a、15bのシフト動作をフィールド単位で交互に開始させ、それぞれの出力をフィールド単位で交互に選択することにより、電子シャッタ動作をフィールド単位で交互に電子シャッタ専用の2個の垂直シフトレジスタ15a、15bに振り分けている。

【0085】この場合、選択された電子シャッタ専用の垂直シフトレジスタ15a、15bは、読み出し用垂直シフトレジスタ2aよりも先行選択を行うものであり、そのタイミングを変化させることにより画素信号の蓄積を行う時間の長短を変化させることが可能になる。

【0086】したがって、電子シャッタ用の垂直シフトレジスタ15a、15bおよび読み出し用の垂直シフトレジスタ2により同一垂直ラインを1フィールド期間に2回選択し、選択画素の信号蓄積時間を制御する可変電子シャッタ動作を行うことができる。

【0087】また、電子シャッタ制御信号がフィールド周期より短い時間間隔で入力されたとしても、既にシフト動作を開始している一方の電子シャッタ専用の垂直シフトレジスタ15aまたは15bのシフト動作が最終段に達する前（読み出し用の全ての画素行の選択を終わらないうち）に途中でリセットされることなく、最後の画素行まで順次選択して選択画素の信号蓄積時間を制御する。

【0088】そして、読み出し用画素行の最終行の選択終了後から次々回のフィールド期間における1行目の読み出し用画素行の選択開始までの期間は第2のダミー画素行142あるいは第3のダミー画素行143を選択制御する。

【0089】また、読み出し用の垂直シフトレジスタ2aは、垂直有効走査期間内の各水平期間には各対応する画素行を選択制御し、垂直帰線期間には第1のダミー画素行141を選択制御する。

【0090】つまり、各垂直シフトレジスタ2a、15a、15bは、それぞれ全ての読み出し用の画素行を選択した後もダミー画素行を選択し続け、後のフィールド期間における選択開始を待機する。

【0091】即ち、上記第2の実施の形態の固体撮像装

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置によれば、フィールド単位で交互に電子シャッタ専用の2個の垂直シフトレジスタに電子シャッタ動作を振り分けることにより、フィールド間で信号蓄積時間を変化させることが可能になる。

【0092】この場合、読み出しの走査時間は一定のままで、信号蓄積時間をフィールド単位で連続的に変化させる電子シャッタ機能を実現することが可能になる。なお、同一フィールド内では、どの選択画素行も信号蓄積時間は同じである。

【0093】このように信号蓄積時間を変化させて可変電子シャッタ動作を行わせる場合に、信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じることを防止でき、出力信号の表示画面における横筋などの画像ノイズの発生を防止することができる。

【0094】また、垂直駆動回路16aは、読み出し用の垂直シフトレジスタ2aおよび2個の電子シャッタ用の垂直シフトレジスタ15a、15bの各出力にそれぞれ対応して1本ずつ（合計3本）の画素行を常に選択駆動しており、常に選択負荷が等しいので、選択負荷の大小による読み出しレベルの変動に起因する表示画面上の横縞の発生を防ぐことができる。

【0095】なお、図1および図2に示した固体撮像装置は、1画素毎に画素信号の読み出しが可能な読み出し回路を備えたCMOS型の固体撮像装置に限らず、水平信号線単位で読み出しを行うCCD（電荷結合デバイス）型の固体撮像装置にも適用可能である。

【0096】＜第3の実施の形態＞図4は、第3の実施の形態の増幅型CMOS固体撮像装置の等価回路を示している。

【0097】図4のCMOS固体撮像装置は、図12を参照して前述した従来例1のCMOS固体撮像装置に対して、例えば受光センサの出力レベルに応じて自動的に信号蓄積時間を変化させることによって等価的に受光時間を変化させる可変電子シャッタ動作をフィールド単位で連続的に変化させることが可能になるように工夫がなされている。

【0098】即ち、図4のCMOS固体撮像装置は、図12を参照して前述した従来例1のCMOS固体撮像装置と比べて、大部分は同様であるが、（1）読み出し用の垂直シフトレジスタ2とは別に2個の電子シャッタ用の垂直シフトレジスタ21、22が付加されている点、（3）2個の電子シャッタ用の垂直シフトレジスタ21、22の動作（信号蓄積時間の制御パルスの出力動作）をフィールド単位で交互に切り換え制御するためのレジスタ切換制御回路（SEL）23が付加されている点、（4）タイミング発生回路10aおよびパルスセレクト回路24の構成が異なり、その他は同じであるので図12中と同一符号を付している。

【0099】即ち、図4において、セル領域（撮像領域）には、例えば4個のトランジスタTa、Tb、T

c、Tdと、1個のフォトダイオードPDから構成される1ピクセル（1画素）／1ユニットの単位セルが二次元の行列状に配置されて形成されている。この場合、各単位セルは、アノード側に接地電位が与えられるフォトダイオードPDと、フォトダイオードPDのカソード側に一端側が接続されている読み出しトランジスタ（シャッタゲートトランジスタ）Tdと、読み出しトランジスタTdの他端側にゲートが接続されている増幅トランジスタTbと、増幅トランジスタTbの一端側に一端側が接続されている垂直選択トランジスタ（行選択トランジスタ）Taと、増幅トランジスタTbのゲートに一端側が接続されているリセットトランジスタTcとを具備する。

【0100】そして、前記セル領域には、各画素行に対応して、同一行の単位セルの各読み出しトランジスタTdのゲートに共通に接続された複数の読取り線4と、同一行の単位セルの各垂直選択トランジスタTaのゲートに共通に接続された垂直選択線6と、同一行の単位セルの各リセットトランジスタTcのゲートに共通に接続されたリセット線7が形成されている。

【0101】また、前記セル領域には、各画素列に対応して、同一列の単位セルの各増幅トランジスタTbの他端側に共通に接続された垂直信号線VLINと、同一列の単位セルの各リセットトランジスタTcの他端側および各垂直選択トランジスタTaの他端側に共通に接続された電源線9が形成されている。

【0102】さらに、セル領域の一端側の外部には、前記垂直信号線VLINの各一端側と接地ノードとの間にそれぞれ接続された複数の負荷トランジスタTLが水平方向に配置されている。

【0103】また、セル領域の他端側の外部には、例えば2個のトランジスタTSH、TCLPと2個のコンデンサCc、Ctから構成された複数のノイズキャンセラ回路が水平方向に配置されている。

【0104】そして、上記各ノイズキャンセラ回路を介して前記垂直信号線VLINの各他端側に接続された複数の水平選択トランジスタTHが水平方向に配置されている。

【0105】上記水平選択トランジスタTHの各他端に共通に水平信号線HLINが接続されており、この水平信号線HLINには水平リセットトランジスタ（図示せず）および出力増幅回路AMPが接続されている。

【0106】なお、前記各ノイズキャンセラ回路は、垂直信号線VLINの他端側に一端側が接続されたサンプルホールド用のトランジスタTSHと、このサンプルホールド用のトランジスタTSHの他端側に一端側が接続された結合コンデンサCcと、この結合コンデンサCcの他端側と接地ノードとの間に接続された電荷蓄積用のコンデンサCtと、前記コンデンサCc、Ctの接続ノードに接続された電位クランプ用のトランジスタTCLPとにより構

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成されており、前記コンデンサCc、Cmの接続ノードに前記水平選択トランジスタTHの一端側が接続されている。

【0107】さらに、セル領域の外部には、セル領域の複数の垂直選択線6を走査的に選択制御するための読み出し用の垂直シフトレジスタ2と2個の電子シャッタ用の垂直シフトレジスタ(ES1)21および(ES2)22、上記3個の垂直シフトレジスタ2、21、22の出力パルスを選択制御してセル領域の各行の垂直選択線6を走査的に駆動するためのパルスセクタ24、前記複数の水平選択トランジスタTHを走査的に駆動するための水平シフトレジスタ3、前記2個の電子シャッタ用の垂直シフトレジスタ21、22の動作(信号蓄積時間の制御パルスの出力動作)をフィールド単位で交互に切り換え制御するためのレジスタ切換制御回路23、各種のタイミング信号を発生するタイミング発生回路10a、前記ノイズキャンセラ回路の電位クランプ用のトランジスタTCLPの一端などに所定のバイアス電位を発生するためのバイアス発生回路11がそれぞれ配置されている。

【0108】前記タイミング発生回路10aは、フィールド周期のタイミング信号φVR、フィールド周期で可変設定される蓄積時間制御用のタイミング信号φES、水平帰線期間に対応するパルス信号φHP、クロックパルス信号φCKが入力する。

【0109】そして、前記タイミング信号φVR入力をバッファ整形して読み出し用の垂直シフトレジスタに供給するためのタイミング信号φVRRを生成し、前記パルス信号φHP入力をバッファ整形して読み出し用の垂直シフトレジスタおよび2個の電子シャッタ用の垂直シフトレジスタ21、22に供給するためのタイミング信号φHPVを生成する。

【0110】また、前記パルスセクタ24に供給するためのタイミング信号φROREAD、φESREAD、φRESET、φADRESを生成し、前記ノイズキャンセラ回路に供給するためのパルス信号φCLP、φSHを生成する。また、水平シフトレジスタ3に供給するためのパルス信号φHを生成する。

【0111】また、フィールド周期のタイミング信号φVRに基づいてフィールド切換制御用のパルス信号φFIを生成し、信号蓄積時間制御用のタイミング信号φESRとともに前記レジスタ切換制御回路23に供給する。

【0112】前記レジスタ切換制御回路23は、フィールド切換制御用のパルス信号φFI入力に基づいてフィールド単位毎に蓄積時間制御用のタイミング信号φESRの供給先を交互に切り換える。この場合、前記電子シャッタ用の垂直シフトレジスタ21に供給する信号蓄積時間制御用のタイミング信号をφESR1、前記電子シャッタ用の垂直シフトレジスタ22に供給する信号蓄積

時間制御用のタイミング信号をφESR2で表わしている。

【0113】図5は、図4中のパルスセクタ24の一例を示す回路図である。

【0114】図5に示すパルスセクタは、読み出し用の垂直シフトレジスタの出力信号RON、2個の電子シャッタ用の垂直シフトレジスタ21、22の各出力信号ES1n、ES2nが入力するとともに、前記タイミング発生回路10aから供給されるタイミング信号φROREAD、φESREAD、φRESET、φADRESが入力し、これらの入力信号の論理処理を行って各種の駆動信号φREADn、φRESET、φADRESnを出力し、セル領域に供給するように論理ゲートにより構成されている。

【0115】即ち、読み出し用の垂直シフトレジスタの出力信号RONが活性状態の時にはタイミング信号φROREADを選択して読取り線駆動信号φREADnとして出力し、2個の電子シャッタ用の垂直シフトレジスタ21、22の各出力信号ES1n、ES2nのいずれかが活性状態の時にはタイミング信号φESREADを選択して読取り線駆動信号φREADnとして出力する。

【0116】また、読み出し用の垂直シフトレジスタの出力信号RON、2個の電子シャッタ用の垂直シフトレジスタ21、22の各出力信号ES1n、ES2nのいずれか1つが活性状態の時には、タイミング信号φRESETを選択してリセット線駆動信号φRESETnとして出力する。

【0117】また、読み出し用の垂直シフトレジスタの出力信号RONが活性状態の時にはタイミング信号φADRESを選択して垂直選択線駆動信号φADRESnとして出力する。

【0118】図6は、図4の固体撮像装置におけるフィールド単位で連続的に変化させることが可能な可変電子シャッタ動作を説明するために、図4中のタイミング発生回路10a、3個の垂直シフトレジスタ2、21、22およびパルスセクタ24の動作例を示すタイミング波形図である。

【0119】ここでは、図4の固体撮像装置が1フィールド=1/30Hz(1フィールドを1フレームとする30フレーム/秒の画像)の撮像システムで使用される場合を示している。

【0120】図6において、φVRはフィールド周期のタイミング信号入力、φESはフィールド周期で可変設定される蓄積時間制御用のタイミング信号入力、φVRRは読み出し用の垂直シフトレジスタに供給されるフィールド周期のタイミング信号、φFIはフィールド切換制御用のパルス信号、φESR1は一方の電子シャッタ用の垂直シフトレジスタ21に1フィールドおきに供給される蓄積時間制御用のタイミング信号、φESR2は

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他方の電子シャッタ用の垂直シフトレジスタ22に1フィールド間隔で供給される蓄積時間制御用のタイミング信号、R0(i)は読み出し用の垂直シフトレジスタR0の出力、ES1(i)は一方の電子シャッタ用の垂直シフトレジスタ21の出力、ES2(i)は他方の電子シャッタ用の垂直シフトレジスタ22の出力である。

【0121】図7は、図6中の1フィールド期間内の電子シャッタ動作の一例を示すタイミング波形図である。

【0122】図7において、ESnは電子シャッタ用の垂直シフトレジスタ21あるいは22のn段目の出力信号、RONは読み出し用の垂直シフトレジスタ2のn段目の出力信号である。

【0123】tHESは、電子シャッタ用の垂直シフトレジスタ21あるいは22のn段目の出力信号ESnが活性状態(“H”レベル)になる1水平期間を示す。

【0124】tHROは、読み出し用の垂直シフトレジスタ2のn段目の出力信号RONが活性状態(“H”レベル)になる1水平期間を示す。

【0125】HBLKは、1水平期間を水平帰線期間と水平有効走査期間とに分けるための制御パルス信号である。

【0126】φCLPおよびφSHはノイズキャンセラ回路に供給されるパルス信号であり、それぞれ水平帰線期間毎に生成される。

【0127】φHは水平選択トランジスタTHに供給されるパルス信号であり、水平有効走査線期間内で水平方向に配置された水平選択トランジスタTHが順次オンになるように生成される。

【0128】φADRES、φRESETおよびφREADは、前記パルスセクタ24から選択画素行に供給されるパルス信号であり、そのうちのφRESET、φREADは、それぞれ信号蓄積動作および信号読み出し動作の際に水平帰線期間内に活性化されるが、φADRESは、信号蓄積動作の際には生成されず、信号読み出し動作の際に水平帰線期間内に活性化される。

【0129】この場合、上記パルス信号φADRESは、後述するような理由により、信号読み出し動作の際の水平帰線期間内に同一行の垂直選択線6を2回選択制御するように、断続的に2回活性状態になるように生成される。

【0130】次に、図6および図7を参照しながら、図4の固体撮像装置の動作を説明する。

【0131】図4の固体撮像装置の動作は、前述した従来例1の固体撮像装置(図12)の動作(図13)と比べて、基本的には同じであるので同じ動作の説明は省略し、以下、主として異なる動作について説明する。

【0132】即ち、図4の固体撮像装置は、電子シャッタ動作を行う際、レジスタ切換制御回路23により2個の電子シャッタ用の垂直シフトレジスタ21、22のシフト動作をフィールド単位で交互に開始させ、それぞれ

の出力をフィールド単位で交互に選択することにより、電子シャッタ動作をフィールド単位で交互に電子シャッタ専用の2個の垂直シフトレジスタ21、22に振り分ける。

【0133】これにより、図6中のフィールド期間tFa、tFbに示すように、信号蓄積時間制御用のタイミング信号φESがフィールド周期より短い時間間隔で入力されたとしても、電子シャッタ専用の垂直シフトレジスタ21および22が同時に動作することが可能になる。

【0134】この場合、最初に発生するタイミング信号φESR1あるいはφESR2により既にシフト動作を開始している一方の電子シャッタ専用の垂直シフトレジスタ21あるいは22のシフト動作が読み出し用の全ての画素行の選択制御を終わらないうちに途中でリセットされることなく、読み出し用の画素行の最後まで順次選択して選択画素の信号蓄積時間を制御することが可能になる。

【0135】換言すれば、読み出しの走査時間は一定のままで、信号蓄積時間をフィールド単位で連続的に変化させる電子シャッタ機能(連続電子シャッター動作)を実現することが可能になる。なお、同一フィールド内では、どの選択画素行も信号蓄積時間は同じである。

【0136】また、図7に示すように、前記水平期間tHESに電子シャッタ用の垂直シフトレジスタのn段目のシフト段の出力信号ESnにより選択制御したn行目の画素行にパルス信号φRESETとφREADが供給され、このn行目の画素行のフォトダイオードPDでそれ以前に蓄積していた信号電荷を増幅用トランジスタのゲートに読み出すことによって、フォトダイオードの信号電荷を零にする。

【0137】この場合、パルス信号φADRESが“L”のままであり、垂直選択用トランジスタはオフのままであるので、前記増幅用トランジスタのゲートに読み出された信号電荷は垂直信号線VLNへは出力されない。

【0138】この後、前記画素行からの信号読み出し動作の際に、前記水平期間tHROにおける水平帰線期間にφRESETが一時的に活性化した後、φADRESが活性化し、さらにφREADが一時的に活性化する。

【0139】この場合、前記φREADが活性状態(“H”レベル)の時に、フォトダイオードとその周辺配線(本例では後述するφADRES配線)との間の容量結合の影響によるノイズの飛び込みが発生しないように、φADRESパルスを信号蓄積動作時と同じ状態となるように一時的に非活性状態(“L”レベル)にし、このφADRESが非活性状態の期間内に前記φREADを一時的に活性化している。

【0140】このような前記水平期間tHROにおける水平帰線期間内における信号読み出し時の動作を詳しく

説明すると、まず、 ϕ RESETによって増幅トランジスタTbのゲート電極を基準電位にリセットした後、 ϕ ADRESを活性状態(1回目)にして前記n行目の画素行の垂直選択トランジスタTaをオン状態とし、この活性期間内にノイズキャンセラ回路に供給するパルス信号 ϕ CLPを活性化し、黒レベルをクランプする。

【0141】そして、 ϕ ADRESが非活性状態の期間内に ϕ READを活性化することによって前記フォトダイオードPDでそれ以前に蓄積していた信号電荷を増幅トランジスタTbのゲートに読み出す。

【0142】そして、 ϕ ADRESを再び活性状態(2回目)にして前記n行目の画素行の垂直選択トランジスタTaを再びオン状態とし、前記増幅トランジスタTbのゲートに読み出されている信号電荷を垂直信号線VLINへ出力する。

【0143】以上の動作により、前記水平期間tHESにおける読取り線駆動信号 ϕ READの活性状態(“H”レベル)の終了時点から前記水平期間tHROにおける読取り線駆動信号 ϕ READの活性化時点までが信号蓄積時間となる。

【0144】図8(a)は、前記ノイズの飛び込みを説明するために、撮像領域の単位セルの一部を取り出して示す平面図である。

【0145】図8(b)は、同図(a)のa-a'線に沿う断面図である。

【0146】図8(c)および(d)は、それぞれ対応して同図(a)中の ϕ ADRESが“L”レベルの時/“H”レベルの時に ϕ READが活性化して信号電荷を読み出す場合の基板内の電位ポテンシャルを示す。ここでは、電源電位が例えば3.3Vである場合を示している。

【0147】図8(a)、(b)において、81はシリコン基板の表層部に形成されたP型ウエル領域、82は基板表層部に選択的に形成された素子分離領域(例えばLOCOS領域)である。基板表層部の素子領域には、フォトダイオードのカソード領域および読み出しトランジスタTdのソース領域を兼ねるn型領域と、読み出しトランジスタTdのドレイン領域となるn型領域(検出ノードDN)が選択的に形成されている。

【0148】上記読み出しトランジスタTdのチャネル領域上には絶縁ゲート膜を介してポリシリコン配線からなるゲート電極(読取り線4の一部)が形成されており、フォトダイオードPDのn型領域の近傍の素子分離領域82上にはポリシリコン配線からなる垂直選択線5およびリセット線7が略平行に形成されている。

【0149】本実施の形態の読み出し動作に際しては、図8(c)に示すように、フォトダイオードPDに隣接する ϕ ADRES配線が“L”レベルの時に ϕ READが活性化して信号電荷を読み出すので、フォトダイオードPDと ϕ ADRES配線との間に存在する結合容量C

aによりフォトダイオードPD下の基板内の電位ポテンシャルが $-V_{Ca}$ だけ引き下げられ、フォトダイオードPDの蓄積電荷 Q_{Ca} が読み出される。

【0150】これに対して、図8(d)に示すように、フォトダイオードPDに隣接する ϕ ADRES配線が“H”レベルの時に ϕ READが活性化して信号電荷を読み出すと、フォトダイオードPDと ϕ ADRES配線との間に存在する結合容量 C_a によりフォトダイオードPD下の基板内の電位ポテンシャルが $+V_{Ca}$ だけ引き上げられる(ノイズの飛び込みとなる)ので、フォトダイオードPDの蓄積電荷 Q_{Ca} が読み出されなくなり、固体撮像装置の出力信号を画像表示装置の画面に表示した場合に黒信号がつぶれて見苦しい画像になる。

【0151】なお、上記第3の実施の形態の固体撮像装置においても、前記第2の実施の形態の固体撮像装置と同様に、(1)前記撮像領域に第1〜第3のダミー画素行を追加し、(2)3個の垂直選択回路2、21、22のシフト段数を本来の撮像用の画素行数+1の段数とし、(3)垂直選択回路2、21、22の出力に基づいて複数の水平方向の制御線群(4、6、7)を選択的に駆動するための駆動信号をパルスセクタ24で生成する際、垂直選択回路2の最終段出力信号の活性化期間は第1のダミー画素行を選択して駆動し、第2の垂直選択回路21の最終段出力信号の活性化期間は第2のダミー画素行を選択して駆動し、第3の垂直選択回路22の最終段出力信号の活性化期間は第3のダミー画素行を選択して駆動するように構成してもよい。

【0152】このような構成により、パルスセクタ24は、読み出し用の垂直シフトレジスタ2および2個の電子シャック用の垂直シフトレジスタ21、22の各出力にそれぞれ対応して1本ずつ(合計3本)の画素行を常に選択駆動するようになり、常に選択負荷が等しいので、選択負荷の大小による読み出しレベルの変動に起因する表示画面上の横縞の発生を防ぐことが可能になる。

【0153】なお、前記第3の実施の形態では、フォトダイオードPDとの容量結合による黒つぶれの問題が生じる周辺配線として ϕ ADRES配線が存在する場合を説明したが、上記周辺配線として ϕ RESET配線あるいはその他の配線が存在する場合にも、これらの配線とフォトダイオードPDとの容量結合による黒信号のつぶれ(黒つぶれ)の問題が生じるおそれがあるので、これらの配線に関しても前記第3実施の形態における ϕ ADRES配線と同様にレベルを制御すればよい。

【0154】即ち、上記したようにフォトダイオードPDに隣接する読み出しゲート配線以外のフォトダイオードPDの周辺配線の印加電圧として、信号読み出し動作時の信号読み出しパルス ϕ READの活性化期間と電子シャック動作時の読み出しパルス ϕ READの活性化期間に同じ電圧を印加することにより、フォトダイオードPDと周辺配線との容量結合によってフォトダイオード

PDから余分な電荷が読み出されないように制御することができ、いわゆる黒つぶれのない再生像が得られる。

【0155】なお、本発明は、以下の第4の実施の形態に述べるような2画素/1ユニットの単位セルのアレイを有する固体撮像装置にも前記各実施の形態に準じて適用可能である。

【0156】＜第4の実施の形態＞図9は、第4の実施の形態の増幅型CMOS固体撮像装置における2画素/1ユニットの単位セルの等価回路を示している。このCMOS固体撮像装置は、単位セルの構成以外は前述した各実施の形態と同様に構成することができるので、以下、主として2画素/1ユニットの単位セルの構成について説明する。

【0157】図9に示す単位セル30は、2個のフォトダイオード31a、31bを有し、この2個のフォトダイオード31a、31bは、各アノード側に接地電位が与えられ、各カソード側はそれぞれ対応して読み出しトランジスタ（シャッタゲートトランジスタ）32a、32bを介して1個の増幅トランジスタ33のゲートに共通に接続される。上記2個の読み出しトランジスタ32a、32bの各ゲートにはそれぞれ読取り線4a、4bが接続されている。

【0158】前記増幅トランジスタ33は、一端側が垂直信号線VLINに接続され、他端側が垂直選択トランジスタ34を介して電源線9に接続（つまり、前記増幅トランジスタ33はソースフォロア接続）されており、上記垂直選択トランジスタ34のゲートには垂直選択線（アドレス線）6が接続されている。

【0159】さらに、前記増幅トランジスタ33のゲートと電源線9との間に1個のリセットトランジスタ35が接続されており、このリセットトランジスタ35のゲートにはリセット線7が接続されている。

【0160】上記構成の2画素/1ユニットの単位セルは撮像領域に二次元の行列状に配置される。そして、前記2本の読取り線（第1の読取り線4aおよび第2の読取り線4b）、垂直選択線（アドレス線）6およびリセット線7は、撮像領域上に水平方向に形成されており、前記垂直信号線VLINおよび電源線9は、撮像領域上に垂直方向に形成されている。

【0161】図10（a）は、図9の2画素/1ユニットの単位セルの平面パターンの一例を示し、そのB-B線に沿う断面構造を図10（b）を概略的に示している。

【0162】図10（a）、（b）において、90はN型シリコン基板であり、その表層部にPウエル91が形成されている。このPウエル91の表層部には、素子分離領域（例えばLOCOS領域）92、一方のフォトダイオード31aのカソード領域および一方の読み出しトランジスタ32aのソース領域となるN型不純物領域9

31、他方のフォトダイオード31bのカソード領域および他方の読み出しトランジスタ32bのソース領域となるN型不純物領域932およびNMOSTランジスタのSDG領域（図には読み出しトランジスタ32a、32bの共通ドレインとなるN型不純物領域94のみ示す）が選択的に形成されている。

【0163】そして、基板表面上にシリコン酸化膜（ゲート絶縁膜）95が形成され、前記LOCOS領域92の底面下にはフィールドイオンインプラ領域96が形成されている。

【0164】97は増幅トランジスタ33のゲート電極を一部に含むポリシリコンゲート配線、98は増幅トランジスタ33のドレイン領域および垂直選択トランジスタ34のソース領域となるN型不純物領域、99はリセットトランジスタ35のソース領域となるN型不純物領域である。

【0165】100はリセットトランジスタ35のソース領域99と増幅トランジスタ33のゲート配線97と2個の読み出しトランジスタ32a、32bの共通ドレイン領域とを接続する配線である。

【0166】読取り線4aは読み出しトランジスタ32aのゲート電極を一部に含むポリシリコンゲート配線、読取り線4bは読み出しトランジスタ32bのゲート電極を一部に含むポリシリコンゲート配線からなる。

【0167】垂直選択線（アドレス線）6は垂直選択トランジスタ34のゲート電極を一部に含むポリシリコンゲート配線、リセット線7はリセットトランジスタ35のゲート電極を一部に含むポリシリコンゲート配線からなる。

【0168】33aは前記増幅トランジスタ33のソース領域と垂直信号線VLINとのコンタクト部、34aは上記垂直選択トランジスタ34のドレイン領域と電源線9とのコンタクト部である。97aは増幅トランジスタ33のゲート配線97と配線100とのコンタクト部、99aはリセットトランジスタ35のソース領域99と配線100とのコンタクト部、99bはリセットトランジスタ35のドレイン領域と電源線9とのコンタクト部、100aは上記配線100と2個の読み出しトランジスタ32a、32bの共通ドレイン領域とのコンタクト部である。

【0169】上記構成の2画素/1ユニットの単位セルの動作は、前記1画素/1ユニットの単位セルの動作と比べて、5個のトランジスタを所定の順序で動作させてフォトダイオードから信号電荷を読み出す基本動作は同じであるが、2個のフォトダイオード31a、31bから異なるタイミングで信号電荷を読み出す点が異なる。つまり、一方のフォトダイオード31aから信号電荷を読み出す時は第1の読取り線4aに“H”レベルの読取り信号を与え、第2の読取り線4bに“L”レベルの読取り信号を与えたままとし、他方のフォトダイオード3

1bから信号電荷を読み出す時は第2の読取り線4bに“H”レベルの読取り信号を与え、第1の読取り線4aに“L”レベルの読取り信号を与えたままとする。

【0170】<第5の実施の形態>ところで、前記したような2画素/1ユニットの単位セルのアレイを有するCMOS固体撮像装置においては、前記したような電子シャッタ機能を持たせない場合でも、2個のフォトダイオード31a、31bから異なるタイミングで信号電荷を読み出す際に前記したようにアドレス線駆動信号を断続的に2回駆動することにより、出力信号を画像表示装置の画面に表示した際の表示画面上の横縞の発生の問題を防止することが可能になる。

【0171】図11は、第5の実施の形態のCMOS固体撮像装置における1フィールド期間の一部分の信号読み出し動作の一例を示すタイミング波形図である。

【0172】図11において、 ϕ RESET、 ϕ ADRES、 ϕ READ1あるいは ϕ READ2は、パルスセレクトから選択画素行に供給されるパルス信号であり、それぞれ信号読み出し動作の際に水平帰線期間内に活性化されるが、 ϕ READ1、 ϕ READ2は異なる水平帰線期間内に供給される。

【0173】ここで、 ϕ READ1が供給される第1の読取り線4aとアドレス線6との距離よりも、 ϕ READ2が供給される第2の読取り線4bとアドレス線6との距離が短く、第1の読取り線4aとアドレス線6との結合容量よりも第2の読取り線4bとアドレス線6との結合容量が大きいため、2個のフォトダイオード31a、31bからそれぞれ読み出される信号電荷に対する影響が異なることに起因して、出力信号を画像表示装置の画面に表示した際の表示画面上の横縞が発生するおそれがある。

【0174】しかし、 ϕ ADRESは、信号読み出し動作の際の水平帰線期間内に同一行のアドレス線6を2回選択制御するように、断続的に2回活性化状態になるように生成され、2個のフォトダイオード31a、31bからそれぞれ信号電荷を読み出す時に ϕ ADRESがそれぞれ“L”レベルになっているので、上記信号電荷読み出し時の影響がほぼ等しくなり、前記したような表示画面上の横縞の発生の問題を防止できる。

【0175】また、本発明は、上記各実施の形態のタイプの固体撮像装置に限らず、光電変換部を積層した積層型の固体撮像装置にも適用可能である。

【0176】

【発明の効果】請求項1およびそれに従属する各請求項の固体撮像装置によれば、電子シャッター動作を行わせる場合に読み出し用垂直シフトレジスタと電子シャッタ用垂直シフトレジスタの負荷の変動を防止でき、出力信号の表示画面に発生する横縞の画像ノイズを抑制でき、S/Nの高い鮮明な画像を得ることができる。

【0177】請求項3およびそれに従属する各請求項の

固体撮像装置によれば、2個の電子シャッタ専用のシフトレジスタにフィールド単位で交互に電子シャッタ動作を振り分けることにより、フィールド単位で信号蓄積時間を変化させる可変電子シャッタ動作(連続電子シャッタ動作)を実現できる。この場合、信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じることを防止でき、出力信号の表示画面における横縞などの画像ノイズの発生を防止することができる。

【0178】特に請求項4の固体撮像装置によれば、請求項3の固体撮像装置と同様に連続電子シャッタ動作を実現できるとともに、2個の電子シャッタ専用の垂直シフトレジスタに対応して2本のダミー画素行を設け、読み出し用のシフトレジスタ、2個の電子シャッタ専用のシフトレジスタにより選択制御される3本の画素行を常に選択駆動することにより、画素行選択に伴う負荷の変動をなくし、表示画面上の横縞の発生を防止できる。

【0179】請求項10およびそれに従属する各請求項の固体撮像装置によれば、電子シャッタ動作を実現できるほか、フォトダイオードに隣接する読み出しゲート以外の周辺配線の印加電圧を、信号読み出し動作時の読み出しパルス信号の活性化期間と電子シャッタ動作時の読み出しパルス信号の活性化期間の両方で同じ電圧とし、配線との容量結合によるフォトダイオードからの余分な電荷の読み出しを抑制することにより、黒つぶれのない再生像が得られる。

【0180】請求項12およびそれに従属する請求項の固体撮像装置によれば、撮像領域の2画素/1ユニットの単位セルにおける2画素の光電変換素子からそれぞれ蓄積電荷を読み出す際、この読み出しを制御する配線に隣接し、前記光電変換素子の周辺に存在する他の配線の電圧を、各画素の読み出し時に実質的に同一にするので、2画素の光電変換素子からそれぞれ信号電荷を読み出す時に他の配線の電圧が及ぼす影響がほぼ等しくなり、表示画面上の横縞の発生の問題を防止できる。

【図面の簡単な説明】

【図1】本発明の第1の実施の形態のCMOS固体撮像装置の等価回路を示す図。

【図2】本発明の第2の実施の形態のCMOS固体撮像装置の等価回路を示す図。

【図3】図2の固体撮像装置において2個の電子シャッタ用垂直シフトレジスタがフィールド単位で交互に電子シャッタ動作を制御する様子を示すタイミング図。

【図4】本発明の第3の実施の形態のCMOS固体撮像装置の等価回路を示す図。

【図5】図4中のパルスセレクトの一例を示す回路図。

【図6】図4中のタイミング発生回路、第1の垂直シフトレジスタ〜第3の垂直シフトレジスタおよびパルスセレクトの動作例を示すタイミング波形図。

【図7】図6中の1フィールド期間内の電子シャッタ動作の一例を示すタイミング波形図である。

【図8】図7に示す電子シャッタ動作においてノイズの飛び込みを抑制する動作を説明するために撮像領域の単位セルの一部について示す平面図、断面図および基板内の電位ポテンシャルを示す図。

【図9】本発明の第4の実施の形態の増幅型CMOS固体撮像装置における2画素/1ユニットの単位セルの等価回路を示す図。

【図10】図9の2画素/1ユニットの単位セルの平面パターンの一例およびその断面構造の一例を概略的に示す図。

【図11】本発明の第5の実施の形態のCMOS固体撮像装置における1フィールド期間内の信号読み出し動作の一例を示すタイミング波形図。

【図12】従来例1のCMOS固体撮像装置の等価回路を示す図。

【図13】図12のCMOS固体撮像装置の動作例を示すタイミング波形図。

【図14】図13中のタイミング発生回路、垂直シフトレジスタおよびパルスセクタの動作例を示すタイミング波形図。

【図15】従来例2のCMOS固体撮像装置の等価回路を示す図。

【図16】図15中の2つの垂直シフトレジスタの行選択タイミングの一例を示す図。

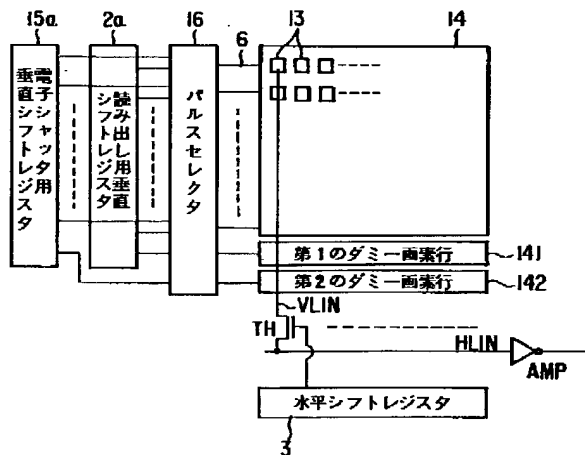
【図17】図15の固体撮像装置において信号蓄積時間

を変化させるために、電子シャッタ用垂直シフトレジスタが読み出し用垂直シフトレジスタよりも先に行選択を行うタイミングを変化させて画素信号の蓄積を行う時間の長短を変化させる場合の問題点を説明するために示すタイミング図。

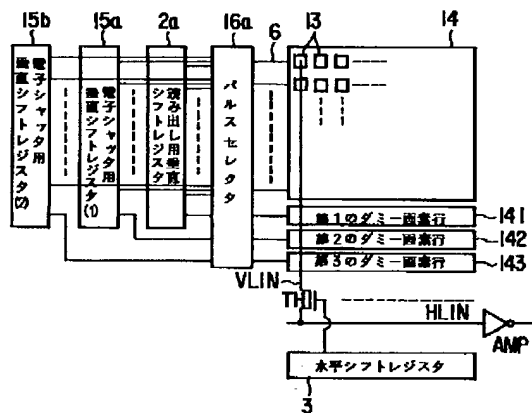
【符号の説明】

- 2…読み出し用の垂直シフトレジスタ、
- 3…水平シフトレジスタ、
- 4…読取り線、
- 10 6…垂直選択線、
- 7…リセット線、
- 9…電源線、
- 10 a…タイミング発生回路、
- 21、22…電子シャッタ用の垂直シフトレジスタ、
- 23…切換制御回路、
- 24…垂直駆動回路（パルスセクタ）、
- PD…フォトダイオード、
- Ta…垂直選択トランジスタ（行選択トランジスタ）、
- Tb…増幅トランジスタ、
- 20 Tc…リセットトランジスタ、
- Td…読み出しトランジスタ、
- TH…水平選択トランジスタ、
- VLIN…垂直信号線、
- HLIN…水平信号線。

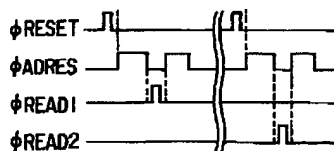
【図1】



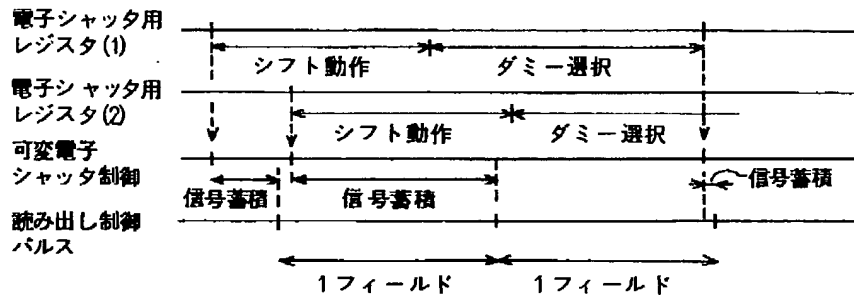
【図2】



【図11】

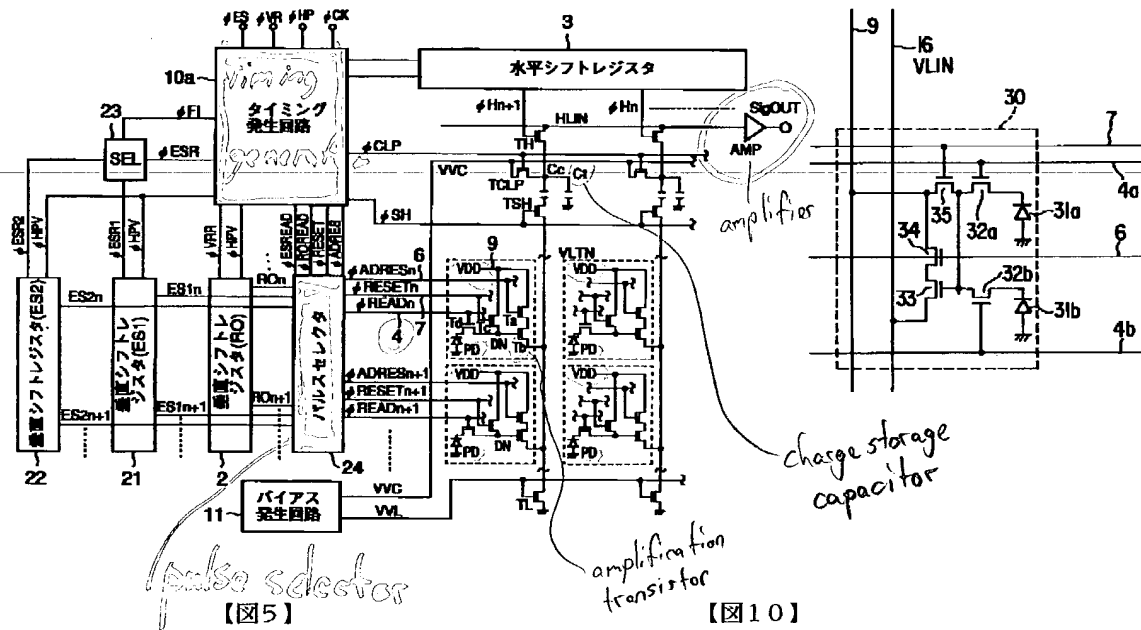


【図3】



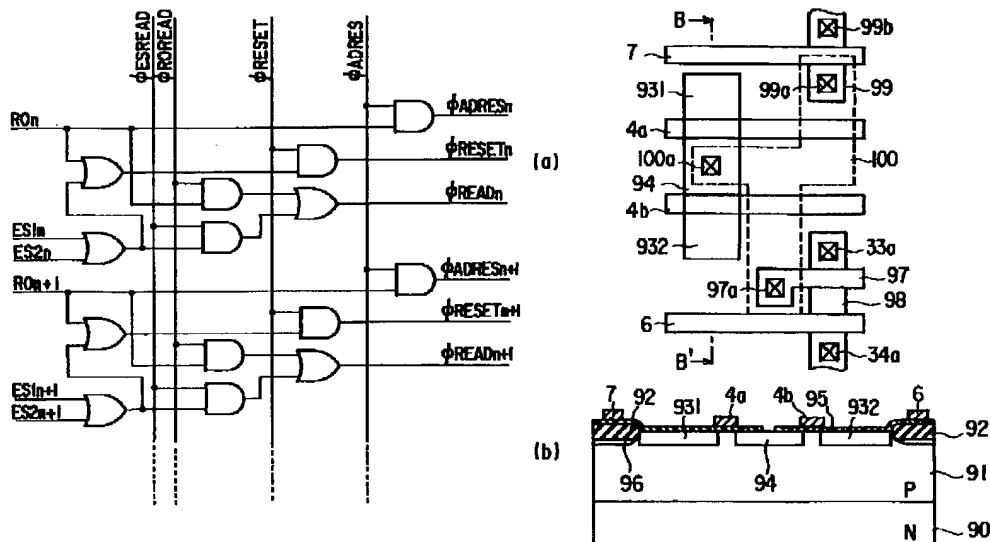
【図4】

【図9】

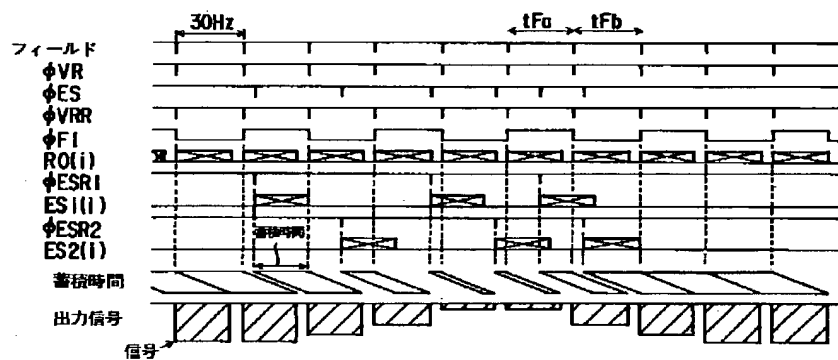


【図5】

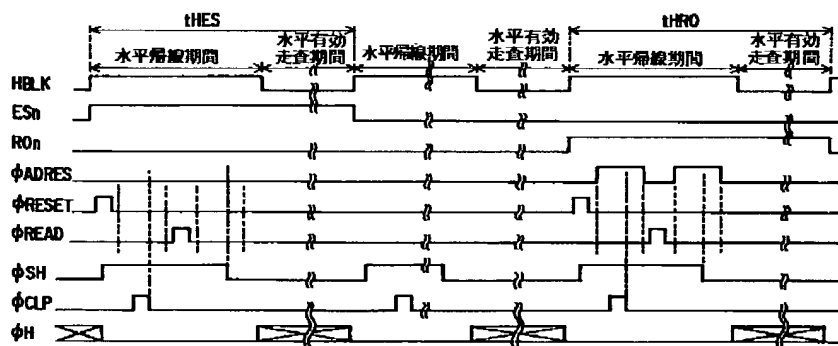
【図10】



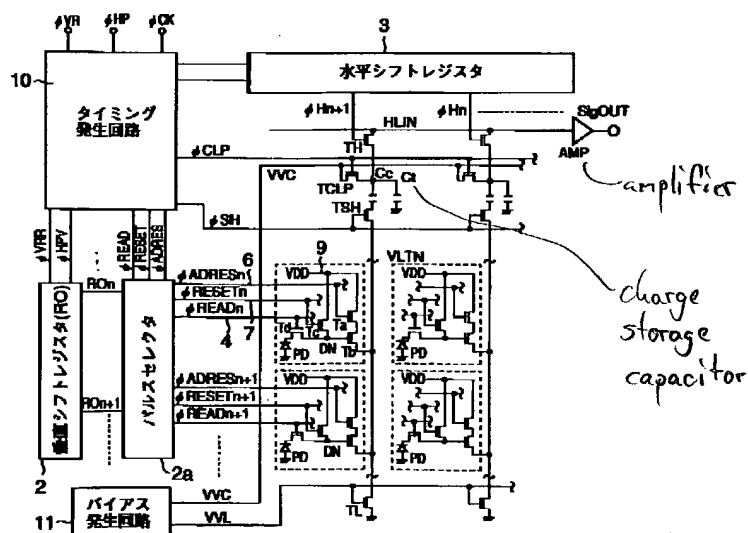
【图7】



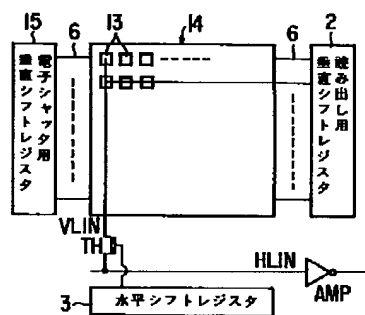
【图7】



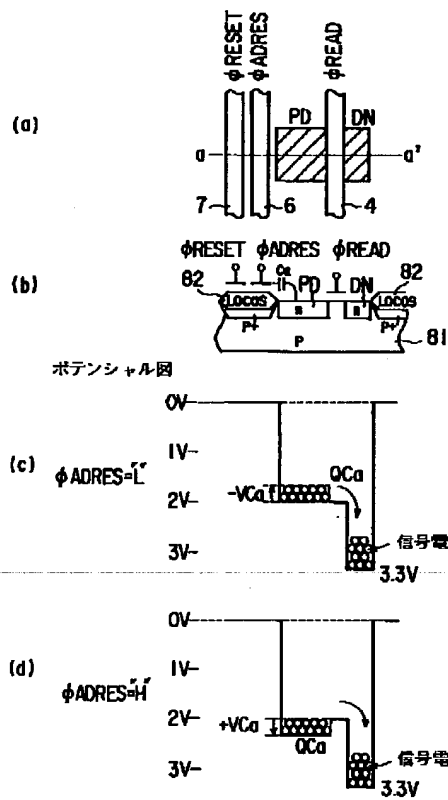
【例 12】



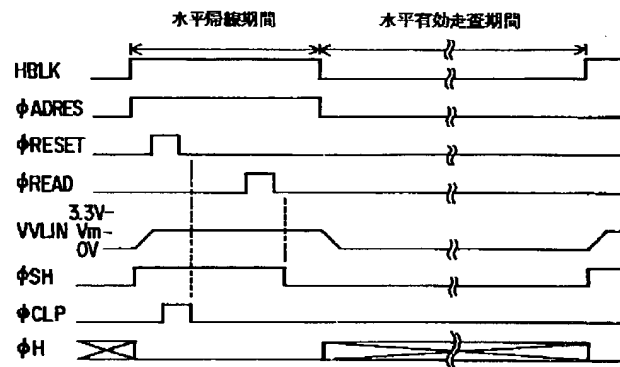
【図15】



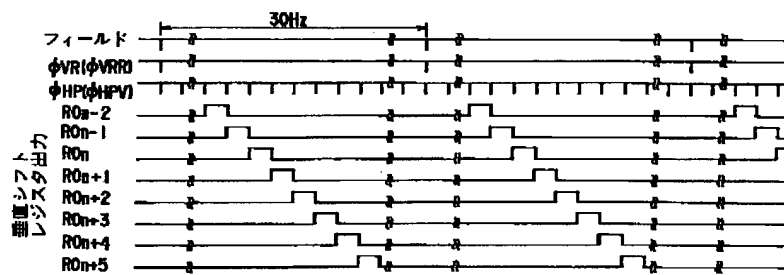
【図8】



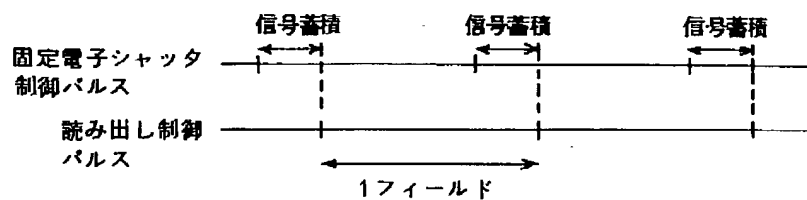
【図13】



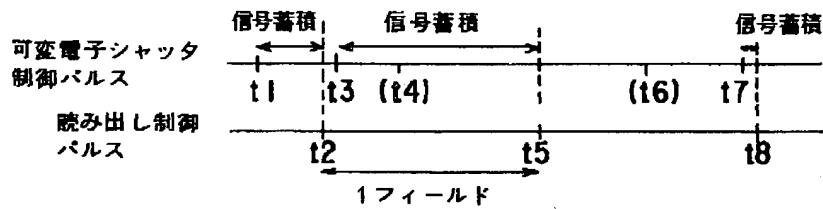
【図14】



【図16】



【図17】



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